

AD-A225 883

Semi-Annual Report

Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures

Supported under Grant #N00014-88-K-0341/P00002
Office of the Chief of Naval Research
Report for the period January 1, 1990-June 30, 1990

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July, 1990

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REPORT DOCUMENTATION PAGE			Form Approved OMB No 0704-0188	
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1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE July, 1990	3. REPORT TYPE AND DATES COVERED Semi-Annual 1/31/90-6/30/90		
4. TITLE AND SUBTITLE Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures			5. FUNDING NUMBERS R&T:212k003---03	
6. AUTHOR(S) Robert F. Davis				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) North Carolina State University Hillsborough Street Raleigh, NC 27695			8. PERFORMING ORGANIZATION REPORT NUMBER N00014-88-K-0341/ P00002	
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) Sponsoring: ONR, 800 N. Quincy, Arlington, VA 22217 Monitoring: Office of Naval Research Resider, N66005 The Ohio State Univ. Research Center 1314 Kinnear Road Columbus, OH 43212-1194			10. SPONSORING / MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES				
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for Public Release; Distribution Unlimited			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) <p>  In this reporting period the RF operation of bipoiar transistors fabricated from a(6H)-SiC have been theoretically modeled and the dc and RF performance of a MESFET fabricated in a-SiC by Cree Research investigated and improved from the standpoints of parasitic resistances and capacitances as well as device design and fabrication procedures. In addition IMPATT diode structures have been further developed, ohmic and Schottky contact materials selected and deposited and the design and construction of a new MBE/ALE system virtually completed. </p>				
14. SUBJECT TERMS alpha SiC, theoretical models, MESFETs, IMPATTs, ohmic, and Schottky contacts, MBE/ALE deposition			15. NUMBER OF PAGES 66	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLAS	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLAS	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLAS	20. LIMITATION OF ABSTRACT SAR	

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I. Introduction

The SiC polytype that currently shows the most promise for high power microwave performance is 6H-SiC. The reason for this choice lies in the high quality and availability of this material more than in its basic electrical properties. For instance, an IMPATT diode relies on operation of a diode in avalanche; while very good avalanche characteristics can now be attained with pn junction diodes in 6H-SiC, no avalanche characteristics have been reported for β -SiC diodes. Likewise, no stable MESFET characteristics have been reported for β -SiC for drain voltages higher than 10 V, while 6H-SiC MESFETs are capable of withstanding drain voltages as high as 100 V. The ability to operate at these higher fields is key to the success of SiC at high frequencies. Because of the excellent crystal quality of 6H-SiC currently being produced by Cree Research, devices fabricated from this material can operate reliably in these high fields.

In order to investigate the suitability of SiC for use in fabrication of high frequency electronic devices, various device types are being modeled in this research program. This investigation is expected to provide guidance regarding device structures most suitable for implementation in this material. Devices currently under consideration include the MESFET, IMPATT diode and Bipolar Transistor. These devices are commonly fabricated from Si and GaAs and are used at microwave and mm-wave frequencies. The material parameters of SiC indicate that this material may allow devices with improved performance to be fabricated. Devices with improved RF output power, in particular, may be possible in SiC.

To achieve the aforementioned devices, as well as other device structures, such that they are operable at or near their theoretical capacity, it will be necessary to improve the ohmic and Schottky contacts to the material and to understand the fundamental science underlying the nature of the interface and its relationship to the electrical properties. A limiting factor in improving performance of SiC based devices is the ability to control the electrical characteristics of metal/SiC contacts. An ohmic

contact, characterized by a low contact resistance and a linear current-voltage relationship, generally is more difficult to obtain due to the need to effectively eliminate any barrier to electron transport. For good rectification properties a large potential barrier between the metal and the semiconductor is desired.

As the above challenges to the advancement of the existing technological base of electronic SiC are being investigated, it is necessary to advance the state-of-the-art, especially in the area of low temperature growth of more perfect thin films. To this end a molecular beam/atomic layer epitaxy (MBE/ALE) system for growth of SiC films by the technique of gas-source molecular beam epitaxy has been designed, purchased, and is currently nearing completion. This deposition system will be used for low temperature growth of monocrystalline SiC thin films, and eventually SiC/AlN solid solutions and SiC/AlN heterostructures.

In this reporting period the RF operation of bipolar transistors fabricated from α (6H)-SiC have been theoretically modeled and the dc and RF performance of a MESFET fabricated in α -SiC by Cree Research investigated and improved from the standpoints of parasitic resistances and capacitances as well as device design and fabrication procedures. In addition IMPATT diode structures have been further developed, ohmic and Schottky contact materials selected and deposited and the design and construction of a new MBE/ALE system virtually completed. The details of this research as well as future plans are given in the following sections.

II. Modeling and Simulation of Electronic Devices Fabricated from SiC (Trew-NCSU)

A. Overview

In this aspect of the research for this period, the RF operation and performance of bipolar transistors fabricated from α -SiC have been simulated, the dc and RF performance of an α (6H)-SiC MESFET fabricated by Cree Research determined, and the dc I-V data used to calibrate a model of the device. The RF operation of the MESFET at 3 GHz was also simulated. Although the fabricated device did not produce RF gain the problem was found to be a very large gate resistance due to thin gate metallization. The RF performance simulations were performed assuming a typical value for gate resistance to determine the RF capability of the device.

B. SiC Bipolar Transistor Investigation Procedure

In order to investigate the RF power performance of bipolar transistors fabricated from α -SiC, simulations using commercially available software were performed. Both the nonlinear simulators *Libra* available from EEsof and *MDS* (Microwave Design System) available from Hewlett-Packard were utilized. These simulators permit the RF performance of devices to be investigated by the use of equivalent circuit techniques. That is, equivalent circuit parameter values are determined for specified bias and operating conditions and then used as input data to the model. The dc and RF circuits and the input RF conditions (input power drive and frequency) must also be supplied. The simulators return RF output power at the fundamental and harmonics. The number of harmonics is a user specified parameter, and for this work was arbitrarily set at ten. This number of harmonics increases execution time, but also increases robustness. Knowledge of the RF output power, along with the defined input power and dc bias conditions permits the RF gain and power-added efficiency to be determined.

Both simulators use essentially the same large-signal model for the BJT and, as might be expected, yielded similar calculated results for the large-signal RF performance. In fact, the most significant difference in the simulators appears to be the algorithm used to determine the harmonic balance between the linear RF circuit and nonlinear device model. The HP simulator appears to be faster than that offered by EEsof, but some of this difference may be due to the machines which are used. The HP simulator will only run on HP machines and was run on a HP 340C computer, which is about a four MIP machine. The EEsof simulator runs on a variety of computers and, for this work, was run on a VAXstation 2000, which is about a 1 MIP machine.

C. SiC Bipolar Transistor Design

The design of a bipolar transistor requires an iterative procedure beginning with assumed geometry and doping concentrations. For this investigation doping densities are selected based upon technologically achievable limits. That is, doping densities are limited to those possible with currently available epitaxial growth and doping technology. An initial estimate for the device geometry can be determined from impedance matching considerations, subject to distributed effects limitations. Since operation at low microwave frequency will allow large device size it is necessary to use multiple emitter fingers. The length of each finger will vary according to the design frequency, but in general will be limited to less than $1/20 \lambda$ where λ is the wavelength of the operation frequency. The layout for a typical interdigitated design is shown in Figure 1. The cross-hatched area indicates the emitter area and the clear area the base area. Note that the interdigitated design results in $n+1$ base fingers where n represents the number of emitter fingers. The device illustrated in Figure 1 has five emitter fingers, but the number of emitter fingers in the actual device will vary inversely with the operation frequency. The length of the fingers used in the device analysis was set to 250 microns, which easily satisfies the $1/20 \lambda$ criterion for

operation at 10 GHz. For operation at 3 and 0.5 GHz, the emitter and base finger lengths could be scaled inversely with frequency.

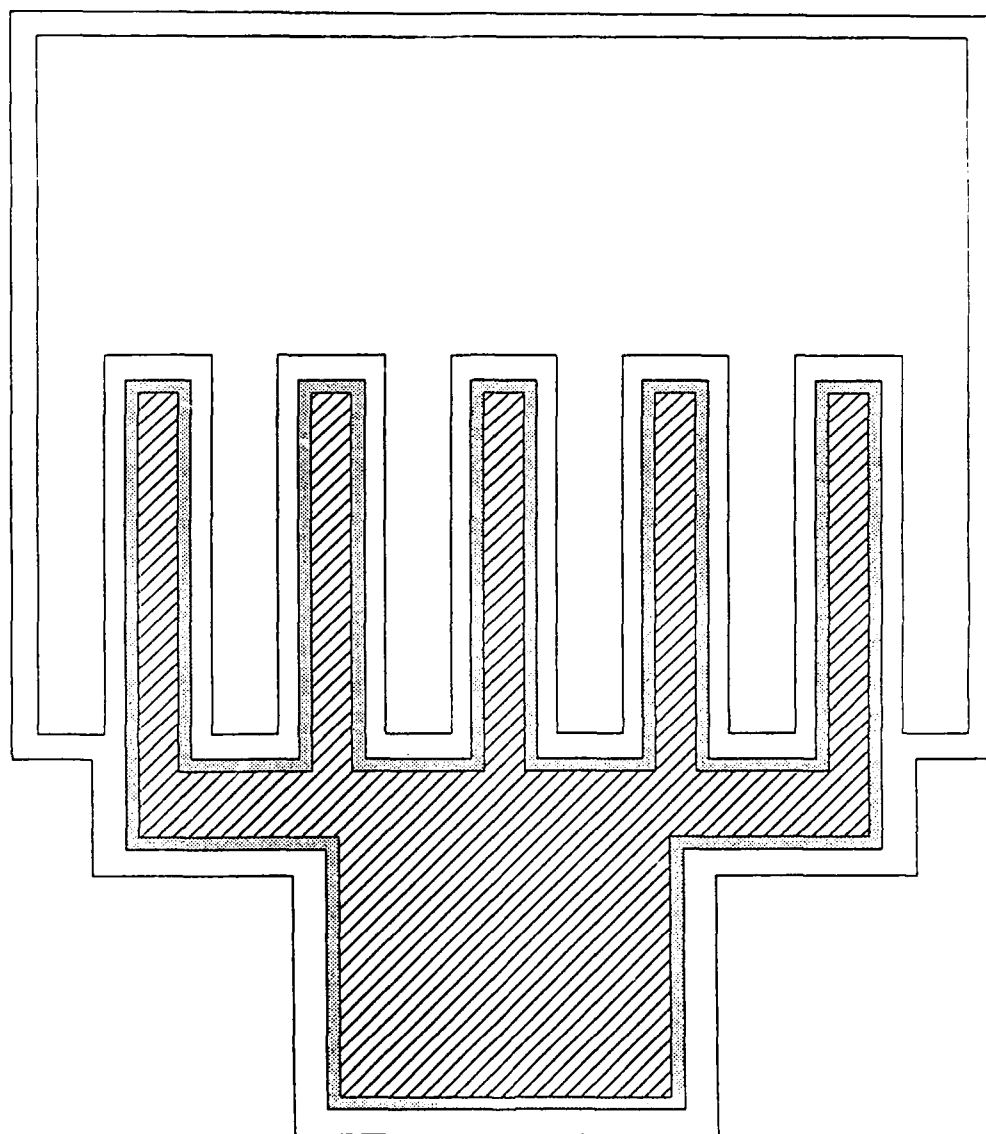


Figure 1. SiC Bipolar Transistor Layout

The cross-section of the final device design is shown in Figure 2, and the design parameters are listed in Table I. This device was designed for 10 GHz operation and has a total of eight emitter fingers. The number of emitter fingers was selected based upon impedance matching and emitter current density considerations. As the base-emitter junction area is increased the input impedance decreases. BJTs

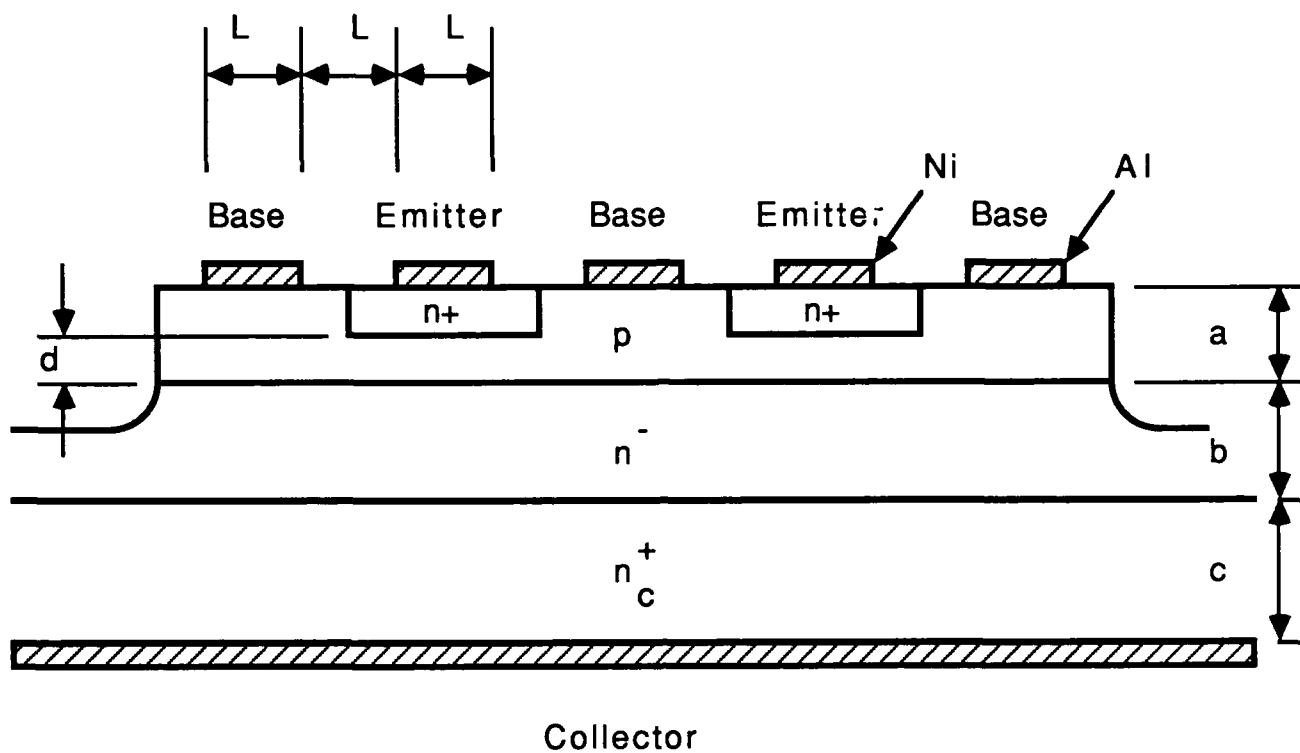


Figure 2. SiC Bipolar Transistor Design

Table I. SiC Transistor Dimensions

Parameter	Dimension
L	2 μm
a	0.5 μm
b	5 μm
c	50 μm
d	0.2 μm
n^+	$2 \times 10^{19} \text{ cm}^{-3}$
p	$3 \times 10^{18} \text{ cm}^{-3}$
n^-	$8 \times 10^{15} \text{ cm}^{-3}$
n_c^+	$4 \times 10^{17} \text{ cm}^{-3}$
$R_c(\text{E})$	$5 \times 10^{-5} \Omega\text{-cm}^2$
$R_c(\text{B})$	$7 \times 10^{-4} \Omega\text{-cm}^2$
$R_c(\text{C})$	$10^{-3} \Omega\text{-cm}^2$

fabricated from SiC, however, will have a relatively large base resistance and this factor will ultimately dominate the input impedance. Under these conditions the device area will be limited by emitter current density and output port impedance matching considerations. It is desirable to keep the device output impedance in the range of 25-50 Ω and the emitter current density in the range of 20-30 kA/cm². These considerations yielded the 8 emitter finger design. The device can easily be scaled for lower frequency operation by an increase in the number and length of the emitter and base fingers.

The most critical design considerations were directed towards the base and collector region. Base region design issues include the conflicting effects of base region resistance and base region transit time. Collector region design issues include base-collector region capacitance (charge storage) and base-collector depletion region transit time. The base region design involves a calculation of the current gain, base resistance, and base region transit-time. The current gain is calculated from consideration of minority carrier transport across the base region. In the common-base configuration the dc current gain is defined as α_0 and is given by the expression

$$\alpha_0 = \frac{1}{\cosh\left(\frac{W_B}{L_B}\right) + \frac{D_{pE}L_BN_B}{D_{nB}L_EN_E}\sinh\left(\frac{W_B}{L_B}\right)}$$

where the various terms are calculated from the design dimensions listed in Table I. Base region transit-time τ_B is also an important factor and this parameter is generally defined in terms of the alpha cutoff frequency for the device defined as

$$f_\alpha = \frac{1}{2\pi\tau_B} = \frac{D_{nB}}{\pi W_B^2}$$

The current gain will degrade with frequency according to the expression

$$\alpha = \frac{\alpha_0}{1 + j \frac{f}{f_\alpha}} e^{-j\omega\tau}$$

where the various terms are indicated in Table I. These expressions indicate the tradeoffs between base region and base-collector region transit-times in determining the current gain for the device.

The base thickness, as indicated in Table I, is $W_B=0.2 \mu\text{m}$. For this base thickness a value of $\alpha_0=0.894$ is obtained, which results in a common-emitter current gain of $\beta_0=8.4$. This is low according to Si BJT standards where α_0 is typically greater than 0.95 and β_0 greater than 20. The parameters listed in Table I yield a base resistance value of 29.7Ω for the 8 emitter finger device. Selection of the base region thickness and doping concentration is a critical design factor for the device. As base region thickness is reduced α_0 increases, but base resistance and base region transit-time increase. An increase in base region doping reduces base resistance, but decreases α_0 and base-region transit-time.

Tradeoffs involved in collector region design are directed towards base-collector region capacitance, C_{BC} , and base-collector depletion region transit-time, τ_C . An increase in collector doping decreases the base-collector depletion region and corresponding transit-time, but increases collector capacitance. An increased collector capacitance lowers output impedance, thereby limiting device area. The base-collector depletion region transit-time introduces an inductive delay that degrades RF performance.

The large-signal equivalent circuit model for the BJT used in this work is shown in the common-emitter configuration in Figure 3. This is a standard model for the bipolar transistor and contains elements of most significance to the RF operation of the device. The calculated parameter values are listed in Table II. Package and lead parasitic elements were added to make the simulations more physical. For this work the common-emitter configuration and class A operating conditions were chosen.

Power devices can be operated either in common-emitter or common-base configurations. A common-base configuration is generally used when the device is limited in RF performance by breakdown voltage considerations. Since SiC demonstrates has a large critical field for breakdown, collector breakdown voltage limitations are not expected to be a factor and for this reason the more desirable common-emitter configuration is selected.

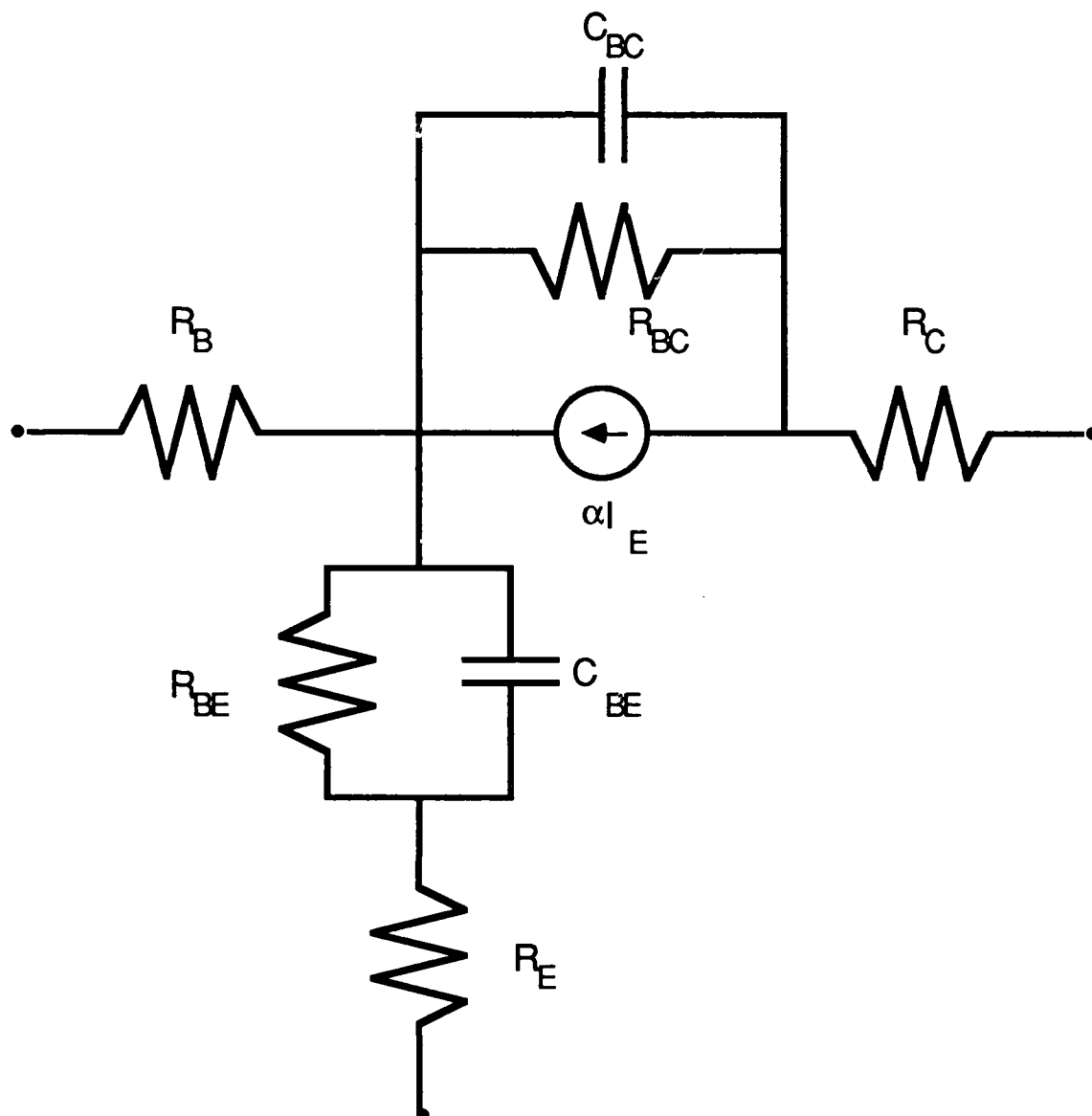


Figure 3. Equivalent Circuit for a Bipolar Transistor

Table II. Element Values

Parameter	Value
No. Emitter Fingers	8
V_{ce}	150 v
I_{ce}	1 A
BV_{ce}	346 v
R_B	29.7 Ω
R_{BE}	0.05 Ω
C_{BE}	15.92 pF
$C_{BE(0)}$	11.93 pF
R_E	2.5 Ω
C_{BC}	0.184 pF
$C_{BC(0)}$	1.5 pF
R_{BC}	250 Ω
R_C	6.4 Ω
α_0	0.894
β_0	8.4
f_α	23.7 GHz
τ_c	23 pS
$\tau_{\text{(minority lifetimes)}}$	10 nS

D. RF Performance Results

The transistor equivalent circuit must be interfaced with an RF circuit and, in order to obtain the optimum performance, the device must be RF tuned based upon a specified criterion. Devices can be tuned for maximum RF output power or maximum power-added efficiency. Typically, these tuning conditions will be performed at an input drive that results in one db compression in the operating gain of the device. Optimized RF power output is obtained under conjugate impedance matched conditions at the output port of the device. Since the input and output impedances of the transistor are a function of drive level the RF circuit required to conjugately match the device varies. The simulators used in this work do not contain routines to determine the optimum impedance information. For this reason, the RF circuit impedance was set for a

conjugate match to the device under linear drive conditions. This will result in a mismatched circuit as the device is driven into saturation and the resulting calculations will under estimate the RF performance. At this time, however, no other technique is available. The calculations do, however, provide a reasonable estimate of the RF capability of the device.

The RF performance of the 8 emitter finger device at 0.5 GHz is shown in Figure 4. The device was operated with a collector bias voltage of 150 v and a collector current of 1 A. Since the collector breakdown voltage for the device is 346 v, high voltage operation is possible. The device produces a maximum RF output power of 57 W, a maximum power-added efficiency of 38%, and a linear gain of 16.5 db. The RF performance of the same device at 3 GHz is shown in Figure 5. At this frequency the device produces a maximum RF output power of 31 W, a maximum PAE of 16%, and a linear gain of 8.5 db. The device did not produce positive gain at 10 GHz. A summary of the RF performance of the device is shown in Figure 6. At frequencies above about 1.5 GHz the RF output power and gain degrade at a -3 db/octave rate, in agreement with the MESFET results. The PAE degrades rapidly with frequency and the device will not produce useful power above approximately 4 GHz. Below 1.5 GHz the RF output power of the device is essentially constant, indicating that the device design is probably not optimum for low frequency operation. At these frequencies the device area could possibly be increased to increase output power. Attempts to design such a device, however, were not successful due to impedance matching problems introduced by increased collector capacitance and conductance with large area devices.

E. SiC MESFET Simulation

The dc and RF performance of the Cree SiC MESFET was investigated. Using the parameter values listed in Table III the dc operation of the device was simulated and a comparison between the simulated and measured I-V characteristics is shown

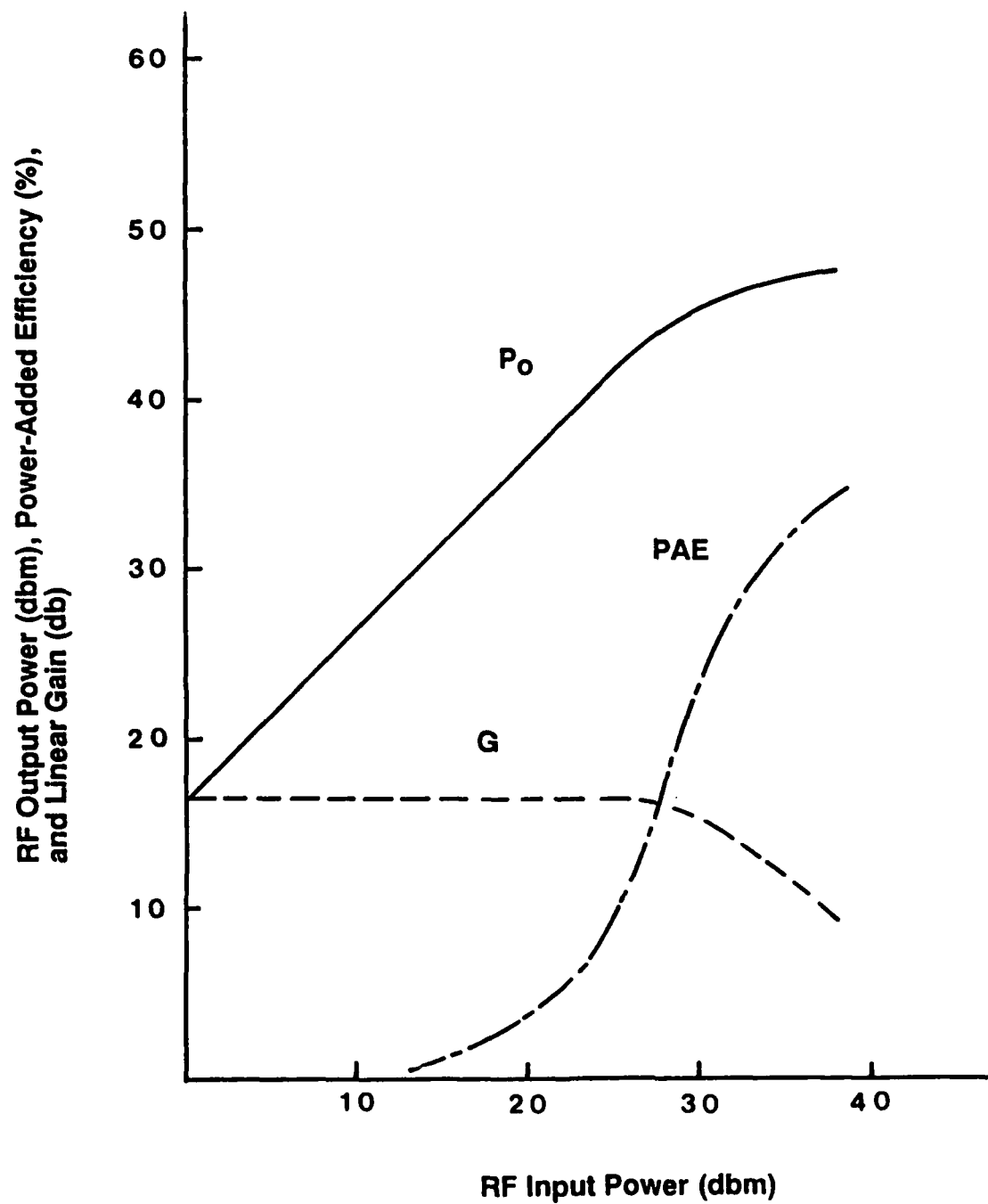


Figure 4. RF Performance for a SiC Bipolar Transistor at 0.5 GHz

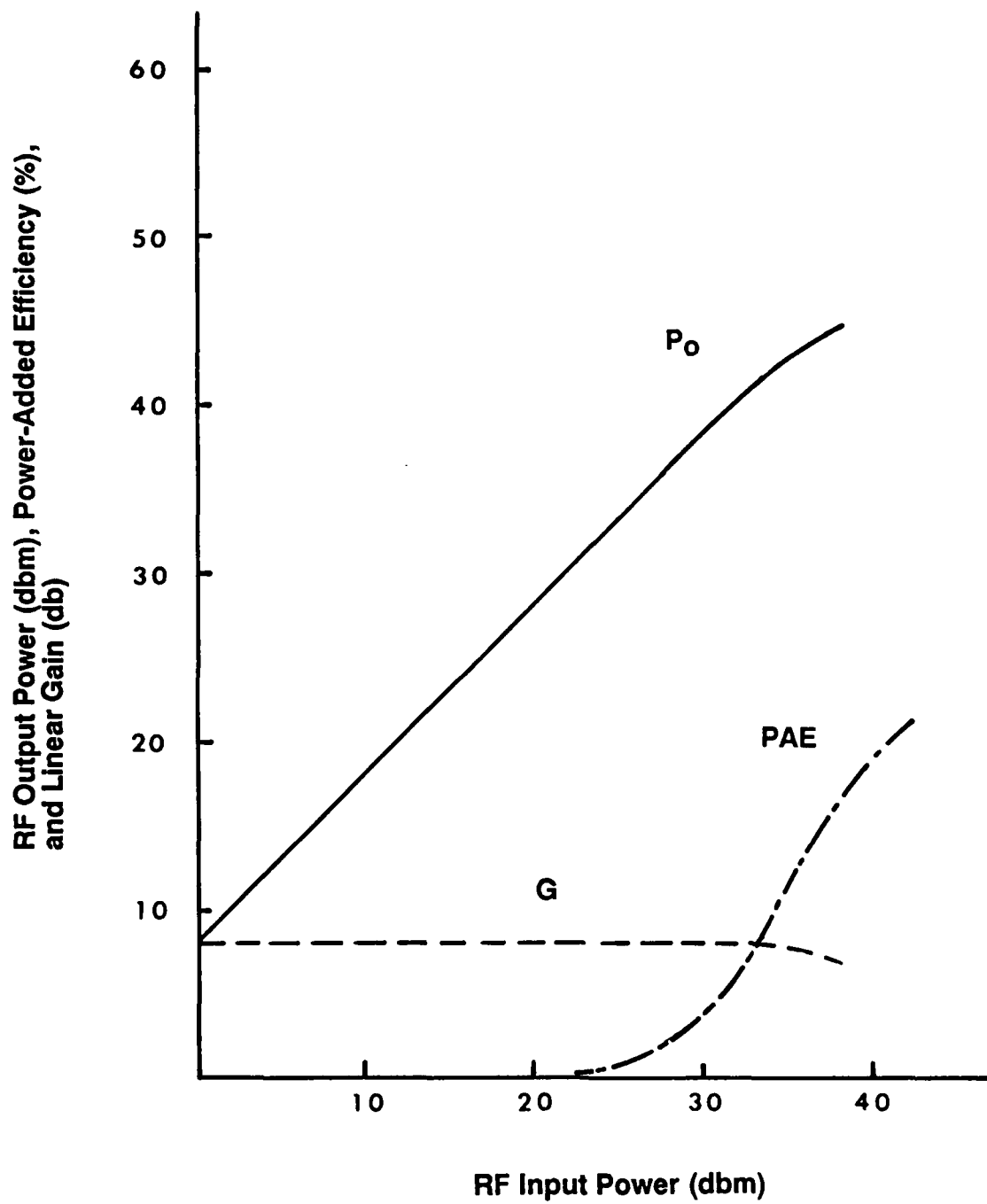


Figure 5. RF Performance for a SiC Bipolar Transistor at 3 GHz

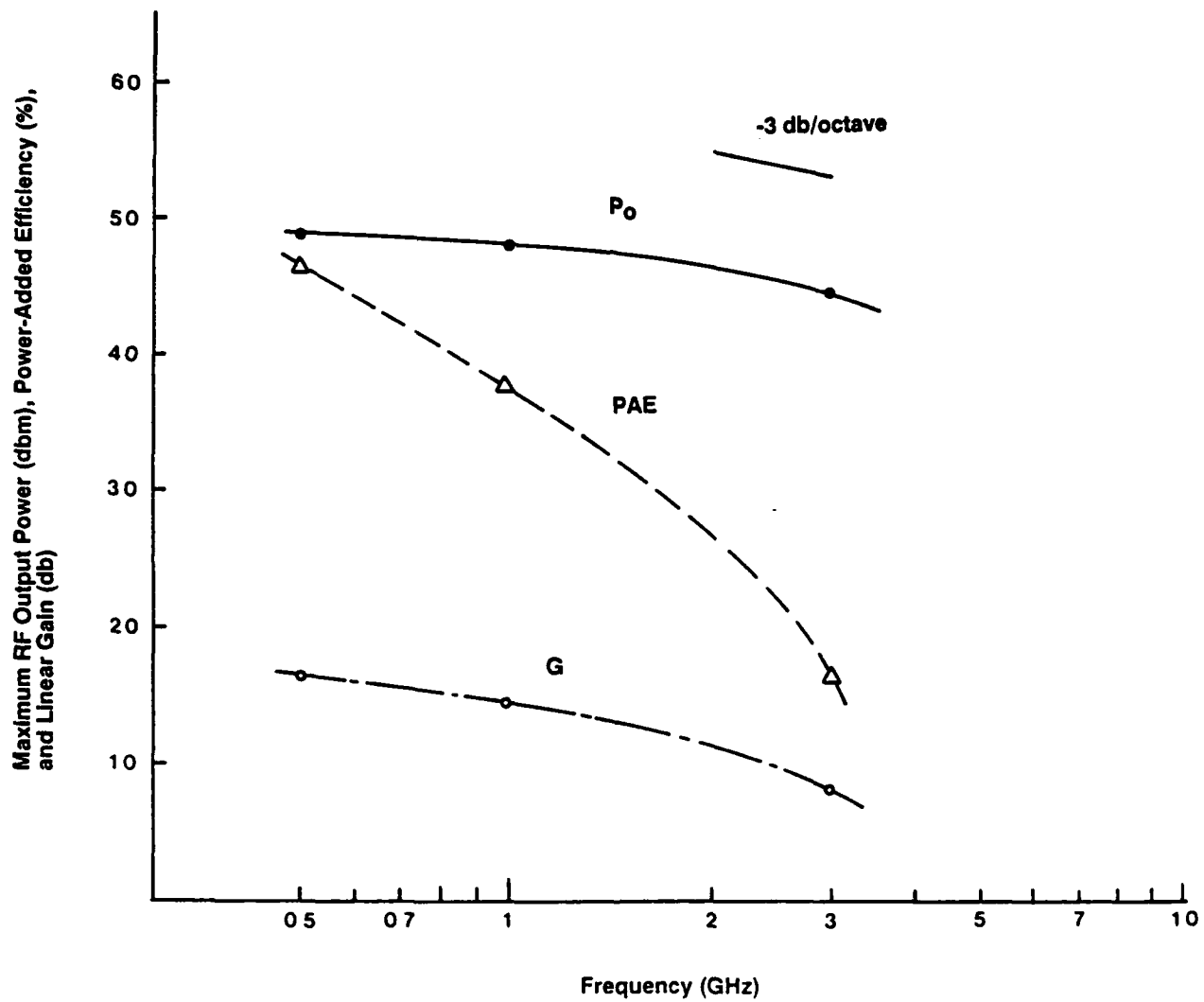


Figure 6. RF Performance versus Frequency for a SiC Bipolar Transistor

in Figure 7. As shown, good agreement between the simulated and measured data is obtained. The measured gate resistance for the device is large (i.e., $R_g \sim 150 \Omega$) and RF gain was not observed with the device, either experimentally or with the simulator. The gate metal, however, is very thin and the gate resistance can be significantly reduced by plating. In order to investigate the expected RF performance the device was simulated with all parameters the same, except for the gate resistance, which was reduced to 2.3Ω . This value is typical of GaAs MESFETs with similar gate length and width. Simulations were also performed for a similar SiC device with the gate length reduced from the current value of 1.75 mm to 1 mm . Improved performance results due to the higher channel electric field. The RF output power, power-added efficiency, and gain at 3 GHz are shown in Figures 8, 9, and 10, respectively. As indicated, very good RF performance should result. The simulations indicate that about 1 W RF power, 22% PAE, and 11 db linear gain should be obtainable from the current device design, if the gate resistance is reduced. A decrease in gate length to $1 \mu\text{m}$ should increase the RF performance to over 1 W , about 30% PAE, and 14 db linear gain.

Table III. SiC MESFET Dimensions

Parameter	Dimension
L_g	$1.75 \mu\text{m}$
W	1 mm
L_{gd}	$1.2 \mu\text{m}$
L_{gs}	$1.2 \mu\text{m}$
a	$0.37 \mu\text{m}$
R_g	1.32Ω
R_{ss}	12Ω
R_{dd}	12Ω

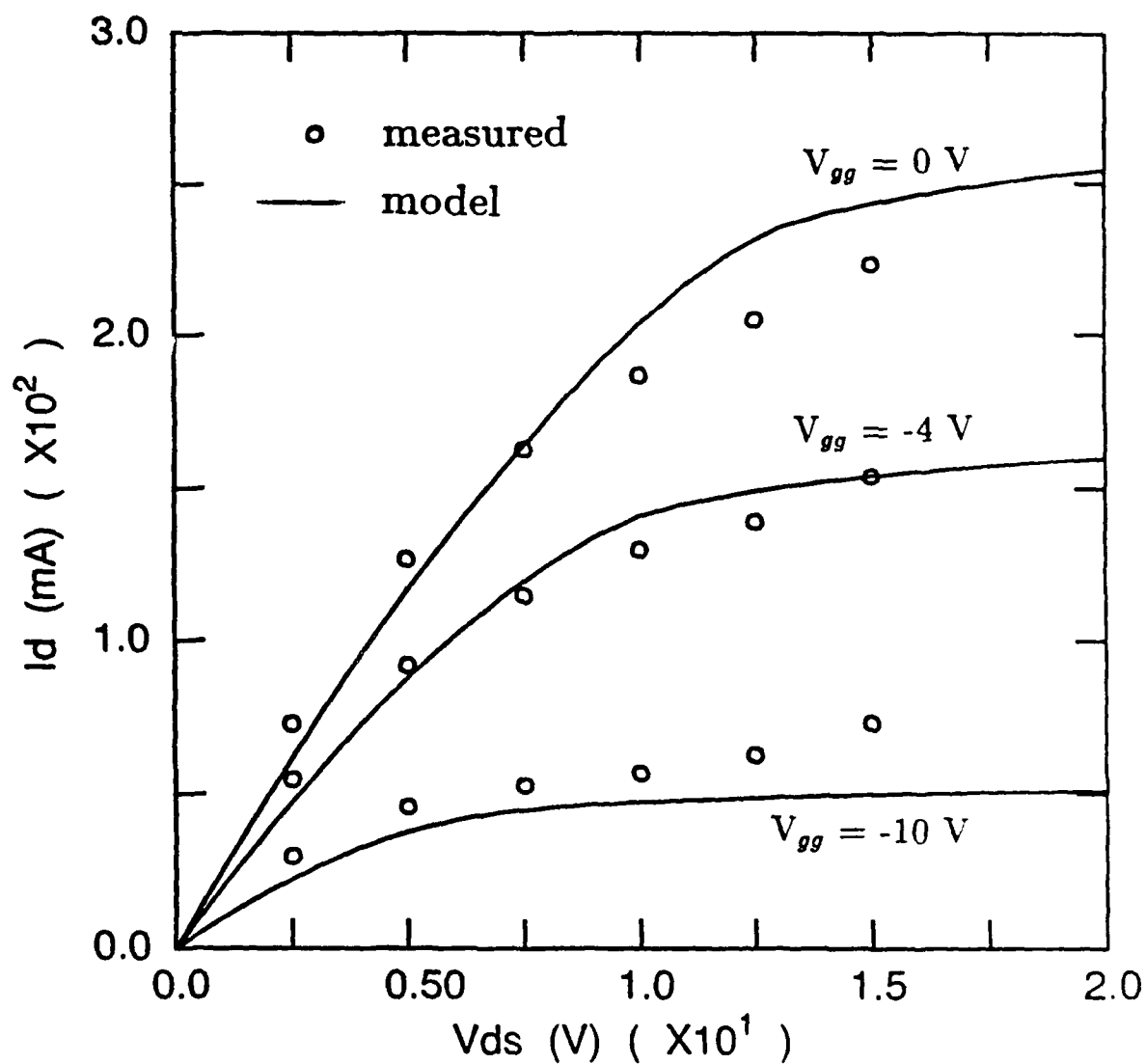


Figure 7. Comparison Between Measured and Simulated I-V Characteristics for a SiC MESFET

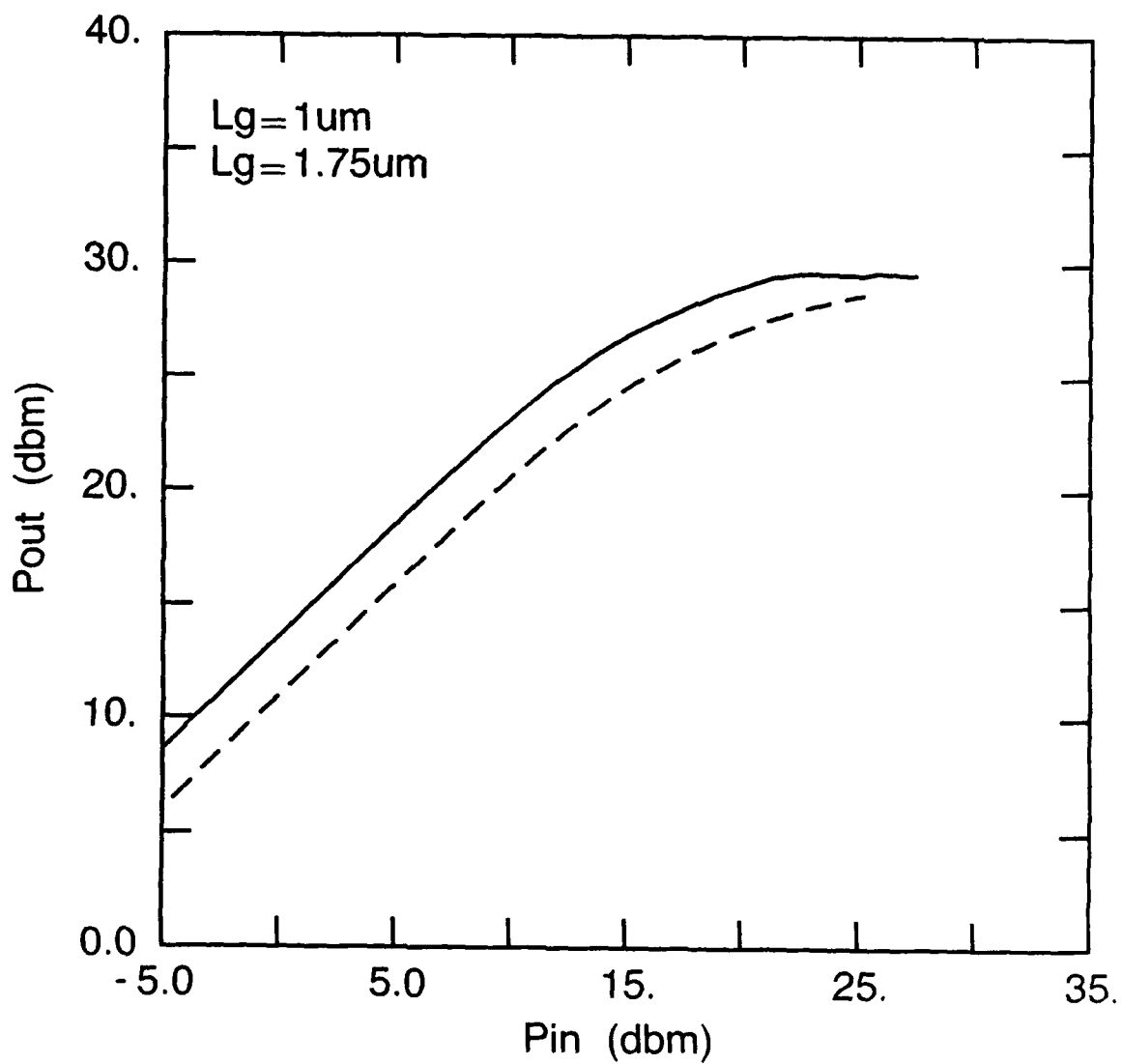


Figure 8. RF Output Power at 3 GHz for the Cree SiC MESFET

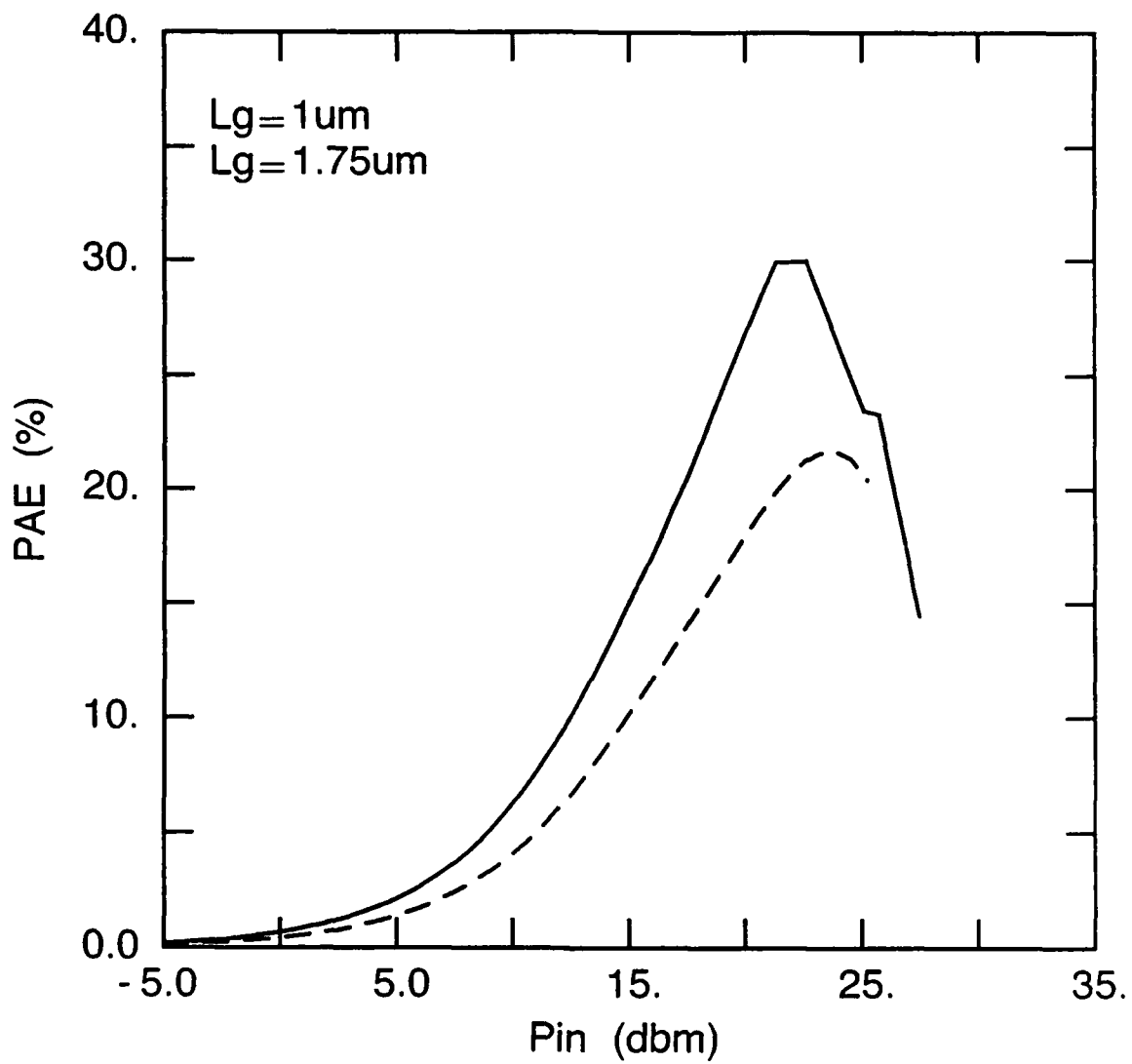


Figure 9. Power-Added Efficiency at 3 GHz for the Cree SiC MESFET

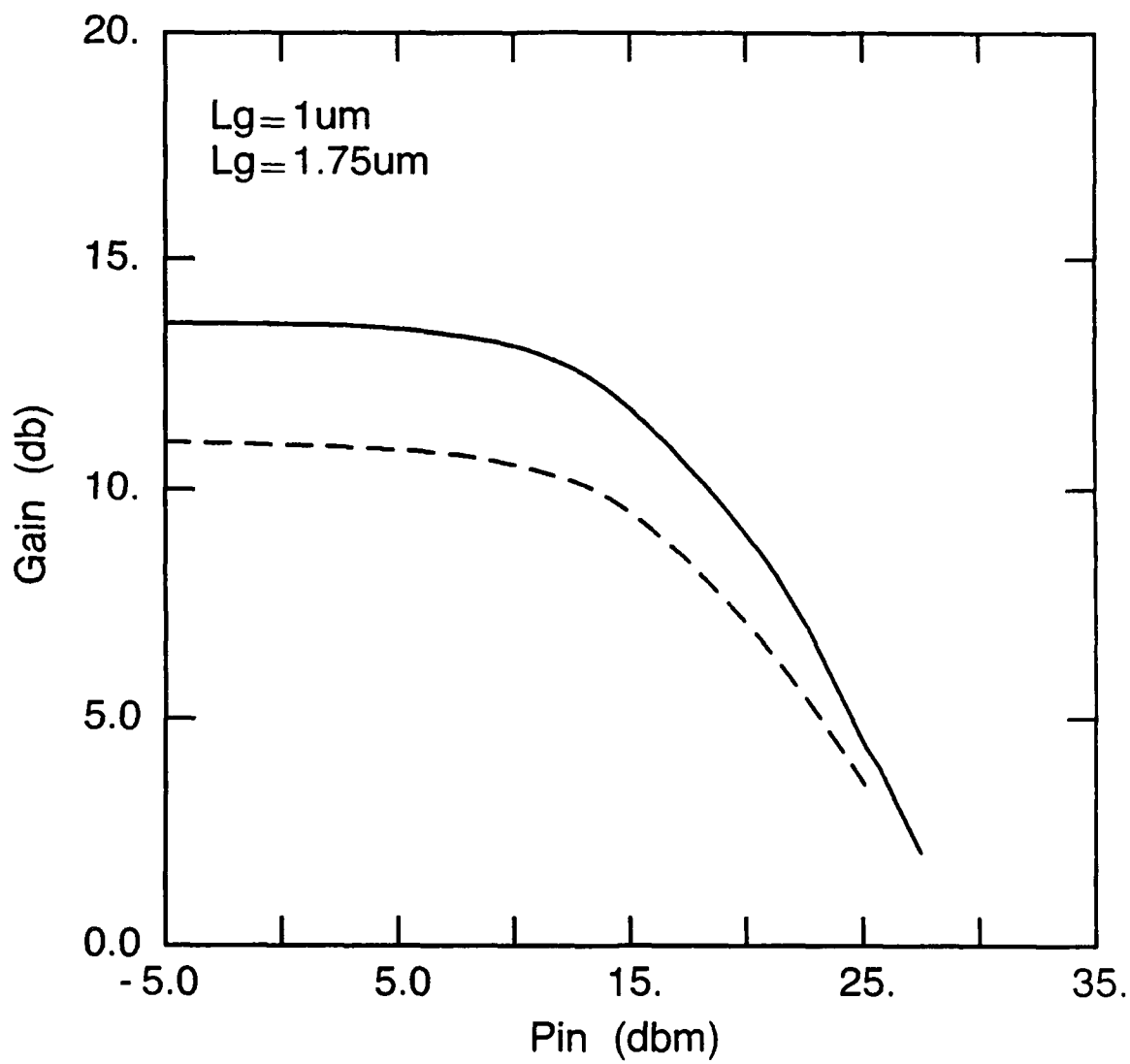


Figure 10. Gain at 3 GHz for the Cree SiC MESFET

F. Summary and Conclusions

The most significant factors limiting SiC BJTs are associated with the base and collector region designs. The low minority carrier mobility in heavily doped SiC results in large base resistance. Although the multiple, parallel base finger geometry helps lower base resistance this parameter is still large. A large base resistance dominates the input impedance and prevents large area devices from being possible. Increased emitter-base area results in low impedance so that almost the entire input voltage appears across the base resistance, rather than the base-emitter junction. Poor gain characteristics result. The poor minority charge carrier transport characteristics in the base region also result in low current gain. This in turn prevents large output voltage from being generated across the output impedance, thereby limiting RF power capability.

The collector region design is also important. High collector doping results in large charge storage effects and low output impedance. This, in turn, limits the allowable device area, thereby limiting RF output power. Also, operation at high collector current produces a large base-collector region conductance that tends to short the device output. This, of course, severely degrades the transistor performance, especially as the operating frequency is increased. A reduced collector doping reduces the charge storage and conductance effects, but increases the base-collector region transit-time. This results in a significant inductive delay, thereby degrading the device frequency performance. This delay is a significant limitation to obtaining RF performance at 10 GHz.

A major limitation to using SiC for high performance BJTs is the difficulty in designing a device that can take advantage of the favorable material characteristics. For example, it is difficult to design the collector of the device so that charge carriers travel at the high saturated velocity. Although such structures can be designed, the resulting depletion region is so long that significant inductive delay is introduced. The

effect of low field mobility is dominant in bipolar transistors and it is very difficult to design structures that can avoid this problem.

Possible solutions to the problems indicated above include the use of β -SiC and/or the use of heterojunctions, possibly between α -SiC and β -SiC. The mobility of β -SiC has been measured to be as high as $650 \text{ cm}^2/\text{V}\cdot\text{sec}$. Greatly reduced base and parasitic resistances would result, with direct improvements in RF performance. This mobility is sufficiently high to allow the material to be used for both bipolar transistors and MESFETs. Base-emitter heterojunctions would allow very heavy base doping without degradation of the base-emitter junction. Further improvements in base resistance would result due to the heavy doping. The heterojunction would allow large injection efficiency and low emitter capacitance. High injection efficiency yields improved current gain, and low emitter capacitance allows large emitter area. These factors would, of course, result in improved RF power performance.

The dc and RF performance of the Cree SiC MESFET was simulated. Good agreement was obtained between the simulated and measured dc I-V characteristics. The device is limited by high gate resistance due to thin metallization. Increasing the gate metal thickness by electroplating should significantly reduce the gate resistance. With reduced gate resistance the simulator predicts that good microwave performance should be obtained. The device should produce about 1 W RF power and 20% power-added efficiency at 3 GHz.

III. Fabrication and Characterization of SiC Devices for Microwave Applications (Palmour-Cree Research)

A. Overview

The importance of high field operation for SiC microwave performance is two-fold. The first is to obtain the high power levels that are desired at high frequency without having to make an inordinately large device. The second reason is to take advantage of the high saturated electron drift velocity (v_{sat}) of SiC ($2.5 \times 10^7 \text{ cm/sec}$) observed at fields above about $1.5 \times 10^5 \text{ V/cm}$, as shown in Figure 11. For a

MESFET operated with a source-to-drain field greater than this value, the transfer characteristics will be dominated more by v_{sat} than mobility, the latter which is quite low in SiC when compared with Si or GaAs. For an IMPATT diode, the high field capability of SiC obviously allows much more power per unit area to be delivered because it would be avalanching at much higher voltages than equivalent Si or GaAs diodes, and the high v_{sat} allows higher frequency operation. Thus, if a high frequency IMPATT diode is to be fabricated in SiC, then reliable avalanche characteristics must first be proven. Once the best configuration for avalanche operation is defined, then an IMPATT diode can be fabricated. These first steps of development for both high frequency MESFETs and IMPATT diodes have been achieved and will be discussed in this report.

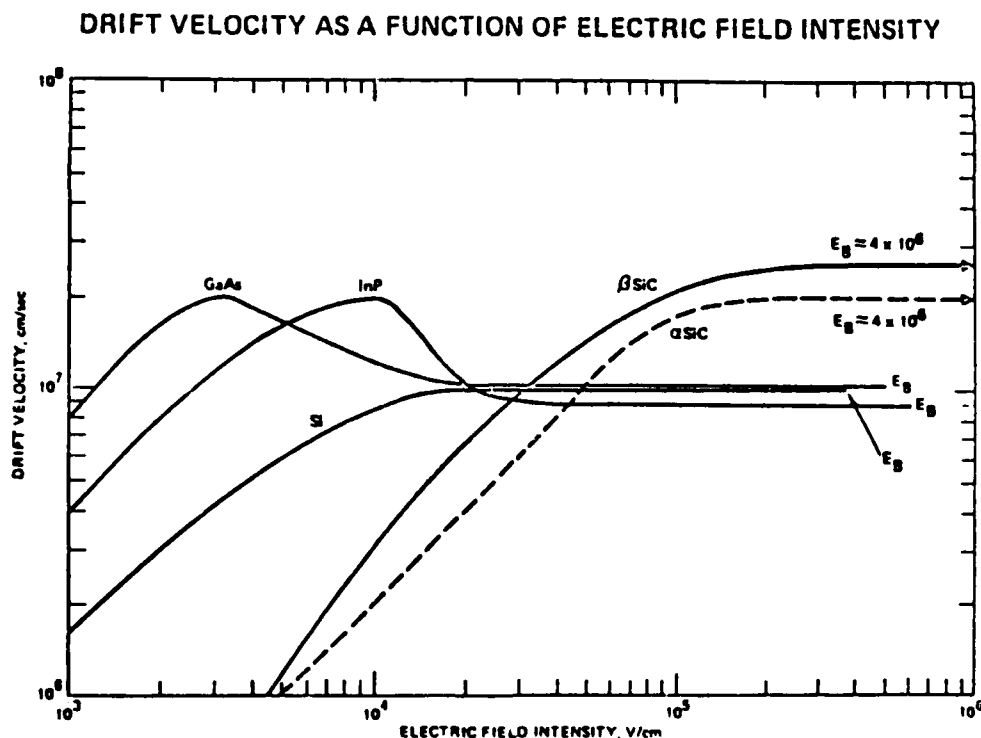


Figure 11: Electron velocity vs. electric field for several semiconductors.

B. Experimental Procedure

Substrate Preparation. The substrates used for this study were sliced from 6H-SiC crystals grown for this project. The crystals were lightly nitrogen doped n-type.

The crystals were then sliced, lapped and polished into wafers suitable for epitaxial growth. The samples used for fabricating MESFETS were n-type epilayers on p-type epilayers, grown on n-type substrates. Each wafer was chemically cleaned prior to device processing.

MESFET Design and Fabrication. Schottky contact samples were first characterized in order to determine the effectiveness of Pt based contacts on 6H-SiC (Pt has been reported to be a very stable Schottky for β -SiC)[1], and to see the effect of carrier concentration on these contacts. The contacts were fabricated by patterning a layer of photoresist such as to leave "doughnuts" of photoresist on n-type epilayers. The Schottky metal, Pt, was then deposited over the entire top surface. The samples were then placed in acetone which dissolved the underlying photoresist and allowed the overlying metal to "lift off" of the doughnuts. This resulted in a series of 100 μm diameter Pt dots, which act as the Schottky contacts, separated from a field of the same metal, which acts as the ohmic contact by virtue of its much larger area.

An interdigitated structure, shown in Figure 12 was used for the initial MESFET design, in order to confirm the high voltage, high power capabilities using the Pt Schottky contact on 6H-SiC. The source consisted of three "fingers" of ohmic contacts on the left, and the smaller area drain consisted of the two fingers of ohmic contacts on the right. Weaving in between these two contacts was the gate or Schottky contact. Isolation trenches were etched in the n-type top conducting layer in order to prevent leakage current around the gate contact between the source and drain. While the gate width was 1 mm for all devices, the gate length and source-to-drain distance was varied in order to determine their effect on transconductance and to be able to extrapolate what the values would be for microwave devices with much smaller dimensions. The different gate lengths were 10 μm , 13 μm , 18 μm and 24 μm , with the source-to-drain distance being 30 μm , 33 μm , 38 μm and 44 μm , respectively.

In cross-section, the device consisted of a 2 μm thick p-type epitaxial layer of

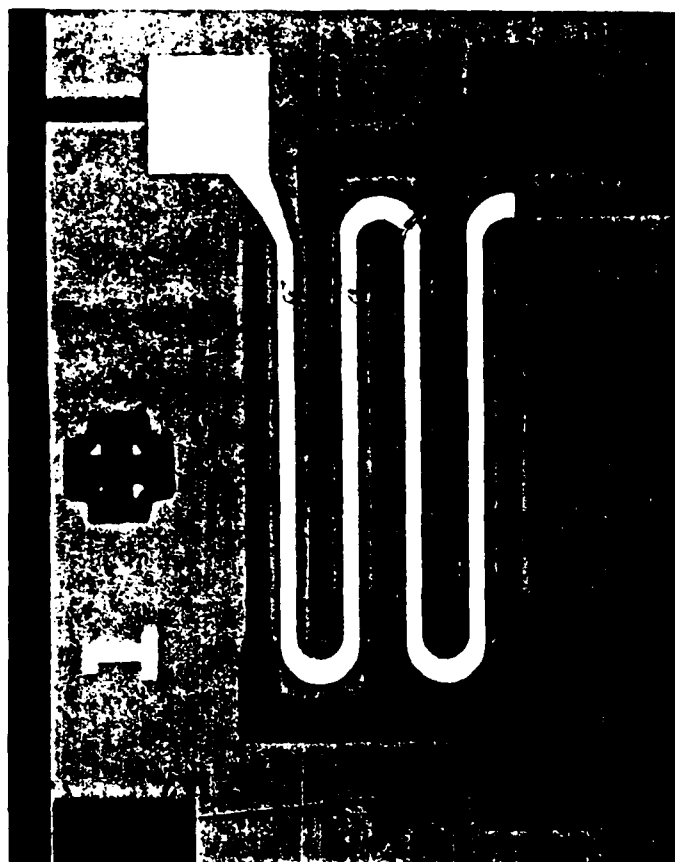


Figure 12: Interdigitated structure of a SiC MESFET. The source contact pad is at the lower left, the drain contact at the lower right, and the gate contact pad is at the upper right. This device has a gate length and width of $10\text{ }\mu\text{m}$ and $1000\text{ }\mu\text{m}$, respectively.

6H-SiC having a carrier concentration in the range of $1 \times 10^{17}\text{ cm}^{-3}$ grown on a 6H-SiC substrate. This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer can have a carrier concentration in the range of $3 \times 10^{16}\text{ cm}^{-3}$ to $3 \times 10^{17}\text{ cm}^{-3}$ and a thickness of 0.2 to $1.0\text{ }\mu\text{m}$ depending on the desired performance of the device.

Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask with which to open windows for the reactive ion etching of the isolation trenches. The trenches were etched deep enough to penetrate through the top n-type layer into the buried p-type

layer. The Al was then stripped, and the sample was oxidized to grow a thin passivating layer of SiO_2 . Windows for the source and drain contacts were then opened in the SiO_2 and the ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the gate Schottky contact was deposited in similar fashion. Unless heat treatment of the gate contact was desired, the device was then ready for measurement.

The initial design of a high power-high frequency SiC MESFET is shown in Figure 13a,b. It consisted consisted of a $2\text{ }\mu\text{m}$ thick p-type epitaxial layer of 6H-SiC having a carrier concentration in the range of $1\text{--}4 \times 10^{16}\text{ cm}^{-3}$ grown on an n-type 6H-SiC substrate (Figure 13a). This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer had carrier concentrations in the range of $7 \times 10^{16}\text{ cm}^{-3}$ to $3 \times 10^{17}\text{ cm}^{-3}$ and a thickness of 0.2 to $0.48\text{ }\mu\text{m}$ depending on the doping and desired pinch-off voltage of the device.

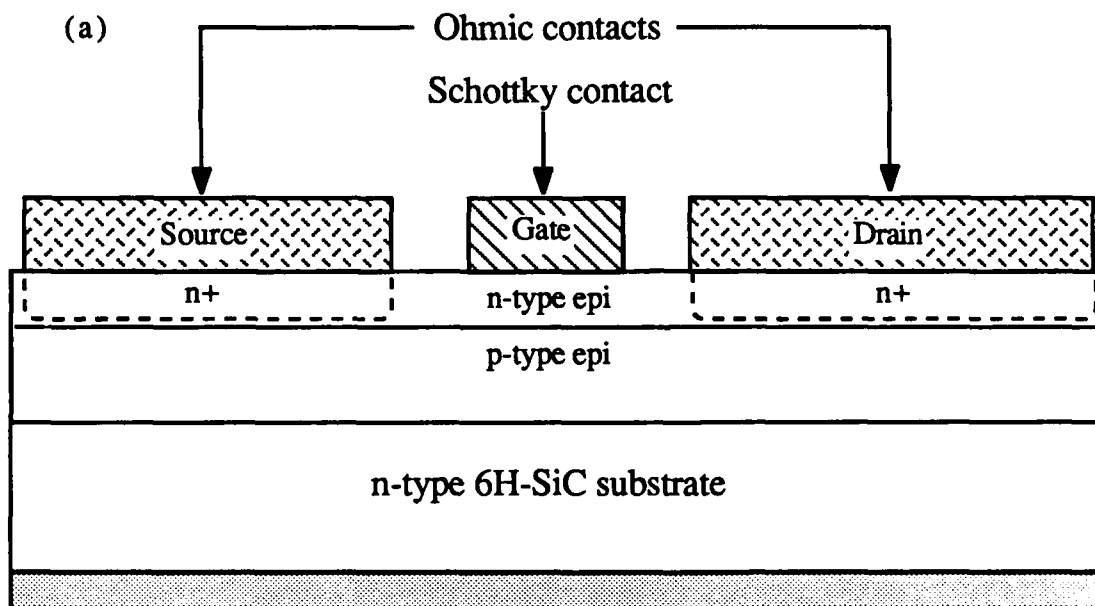
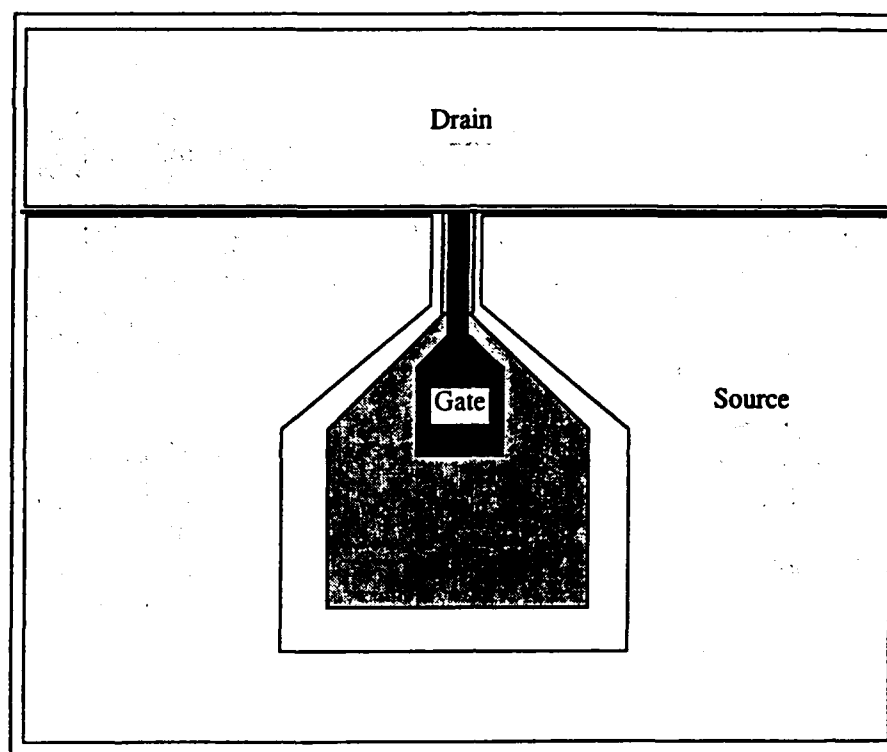


Figure 13. (a) Cross-sectional view 6H-SiC MESFET design utilizing ion implanted n^+ source and drain wells, and a buried p-type isolation layer; (b) Initial design of high power, high frequency SiC MESFET. Gate lengths vary from $4\text{ }\mu\text{m}$ to $0.8\text{ }\mu\text{m}$, and source-to-drain distances vary from $7\text{ }\mu\text{m}$ to $2\text{ }\mu\text{m}$. The gate width is 1 mm .

(b)



The device also had large area source and drain contacts in order to reduce the contact resistance, and the source-to-drain distances range from 7 μm down to 2 μm . The gate contact lengths range from 3 μm down to 0.8 μm . The gate width is 1 mm for all of the devices. The entire device is isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask for the reactive ion etching of the isolation mesa. The material around the mesa was etched deep enough to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped, and polysilicon was deposited and patterned, opening windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed and the samples were oxidized to grow a thin passivating layer of SiO_2 . In order to reduce gate capacitance, 300 nm thick layer of Si_3N_4 was then deposited over the oxide and

patterned to form the center gate contact isolation pad. Windows for the source and drain contacts were then opened via reactive ion etching the nitride and then etching the SiO_2 . The ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the fine line gate Schottky contact was deposited in similar fashion. The patterned gate consisted of only the gate "stripe" with a small $20\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ tab coming off of it, making the actual area of the Schottky contact very small. Contact was then made to the gate by patterning a metal pad on top of the nitride with a strip that drops over the nitride step and overlaps the gate tab. This step reduced the gate capacitance to about 4-6 pF.

One batch of wafers was fabricated in a different manner in an attempt to further reduce the channel resistance and give a self-aligned gate. The wafers had a similar n-channel layer, except it was twice as thick as usual. An Al masking layer was then patterned with the gate line pattern, opening a window for the gate contact. The underlying channel layer was thinned to the desired thickness using reactive ion etching such that the only resistive part of the channel was directly under the gate. The gate contact metal was then deposited over the mask layer. The gate was patterned by subsequently etching the masking Al, thus providing a "lift-off" effect for the gate metal. Unfortunately, there were a variety of fabrication difficulties that arose during this process, and it was eventually deemed to be too difficult to be successfully completed.

IMPATT Diode Design and Fabrication. The initial modeling for IMPATT diodes was for operation at 60 GHz using a flat profile for the drift layer, and showed that this epilayer must have $n = 4 \times 10^{16}\text{ cm}^{-3}$ and a thickness of $2\text{ }\mu\text{m}$. This thickness and carrier concentration are dictated by that desired frequency. Unfortunately, the carrier concentration in turn dictates that the avalanche will occur at voltages in the range of 350-400 V for SiC. This is a demanding voltage from the aspect of junction quality and passivation. While these voltages have certainly been achieved for SiC pn

junction diodes, it requires special structures and passivation techniques that may not readily transfer into a desirable IMPATT fabrication scheme. Therefore, more modeling was performed so that a "high-low" structure could be used, in which the avalanche takes place at a relatively low voltage in a more heavily doped layer, and the drift takes place in a lightly doped layer. The modeling showed the most desirable doping profile for a high-low structure to be a 0.2 μm thick "high" layer with $n = 4.5 \times 10^{17} \text{ cm}^{-3}$, and a 1.2 μm thick "low" layer with $n = 3 \times 10^{16} \text{ cm}^{-3}$. Both the "flat" profile and the "high-low" structure were fabricated. Regardless of the breakdown structure, the same set of masks were used. Seven different diameter dots, varying from 38.1 μm to 381 μm , were designed in order to find the device area that yielded the best impedance matching.

These first IMPATT structures were based on pn junction diodes. The initial design for SiC IMPATTs used a mesa pn junction structure with a passivated sidewall. A variety of epilayer structures were grown so that the best configuration could be determined. Both p^+-n and n^+-p flat profiles were fabricated, as well as the $p^+-n^+-n^-$ high-low structure discussed above. The epilayers were all grown on n^+ substrates for maximum conductivity, and then mesas were reactive ion etched in the SiC to a depth of 14 μm . The sidewalls were passivated via thermal oxidation, and the p-type ohmic contacts were defined and annealed on top of the mesas. The substrates were then thinned to about 60 μm thick, and ohmic contacts were deposited on the backside of these wafers, which were subsequently annealed.

None of these structures showed promising avalanche characteristics, because of the amount of sub-avalanche reverse bias leakage current. Most of the devices had a leakage current of about 1 mA at a reverse bias of 30 V, which was well below the avalanche voltage. For an IMPATT structure, it appears that it will be achieved most easily using the "high-low" structure, which will keep the avalanche voltage low and will decrease the sidewall passivation requirements. These "high-low" structures can be made using either a pn junction diode or a Schottky diode. Both of these structures

will be fabricated during the next reporting period, with the emphasis on reducing the reverse bias leakage current and improving the avalanche current handling capability.

C. Results and Discussion

MESFET Characterization. An I-V curve of one of these SiC MESFETs at room temperature is shown in Figure 14(a). This device had a gate length of 13 μm , a gate width of 1 mm, and a source to drain distance of 33 μm . The device shows good current saturation to $V_D = 40$ V, although there is some non-uniformity at the intermediate gate voltages. The maximum transconductance was 1.5 mS/mm and the threshold voltage is -4.4 V. The subthreshold leakage is quite low, having a value of 44 μA at $V_D = 40$ V and $V_G = -6$ V. The MESFET's I-V characteristics actually improved when heated to 100°C, as shown in Figure 14(b). The maximum transconductance increased to 1.65 mS/mm, and the current saturation was quite good to $V_D = 30$ V, with some leakage still present at higher drain voltages. The subthreshold leakage current was 52 μA at $V_D = 40$ V and $V_G = -6$ V. When heated at 200°C, the I-V characteristics were virtually identical to those shown at 100°C. The I-V characteristics at 300°C are shown in Figure 14(c). The subthreshold leakage increased to 96 μA at $V_D = 40$ V and $V_G = -6$ V, and the maximum transconductance decreased to 1.26 mS/mm, but overall these were promising characteristics. While these particular devices also operated at 400°C, they were unfortunately ruined by holding at this temperature for too long in air. However, it is assumed that if the device was hermetically sealed in a package containing an inert atmosphere, that the devices would have operated to much higher temperatures, indicating that high power MESFETs will withstand a large amount of self-heating.

Improved control over doping and crystal quality led to the fabrication of MESFETs with improved high voltage capability, as shown in Figure 15. This device had a source-to-drain distance of 44 μm and a gate length of 24 μm . Drain voltages of 100 V were achieved without breakdown or significant leakage. The current levels

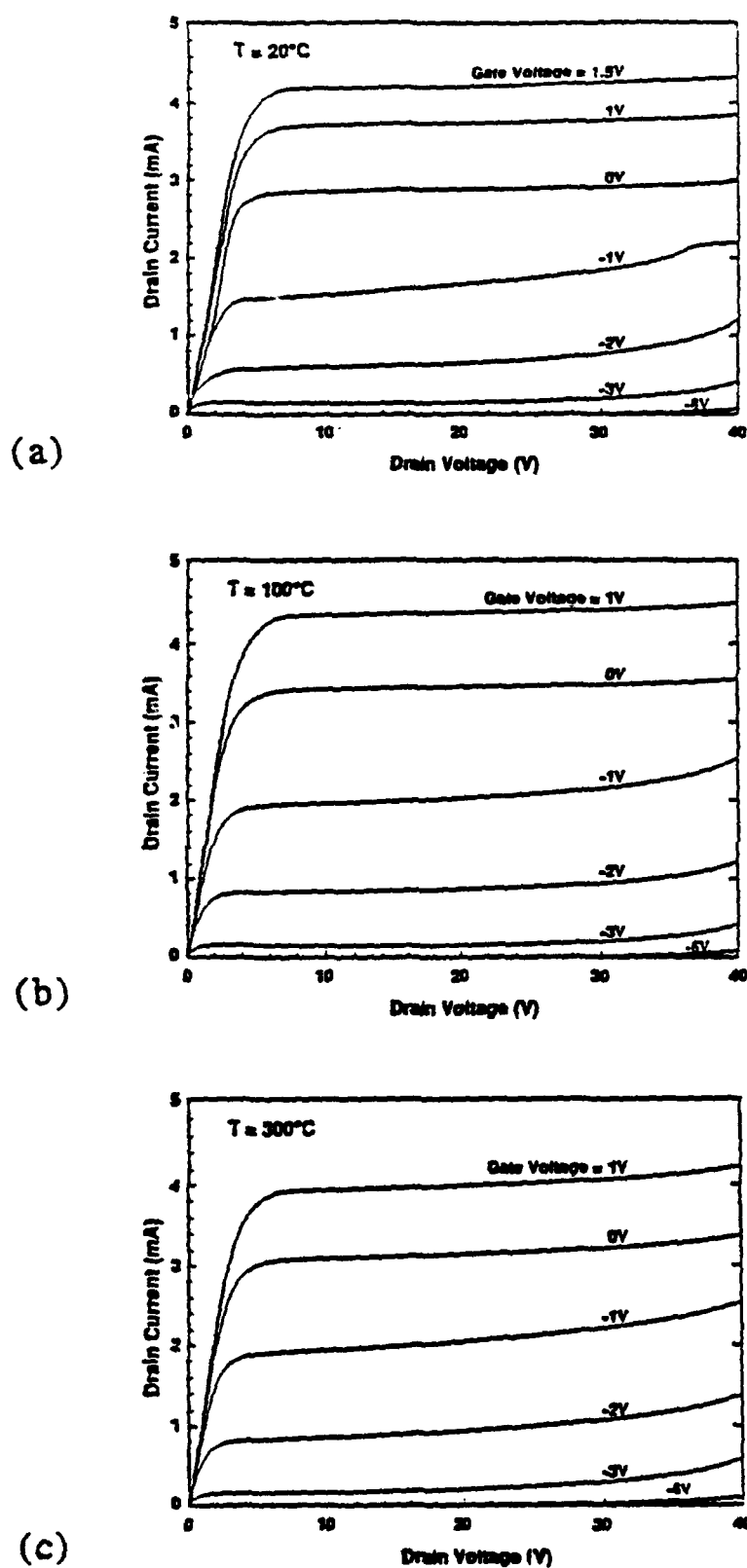


Figure 14. Drain current-voltage characteristics, after an anneal, of a SiC MESFET at (a) 20°C, (b) 100°C, and (c) 300°C.

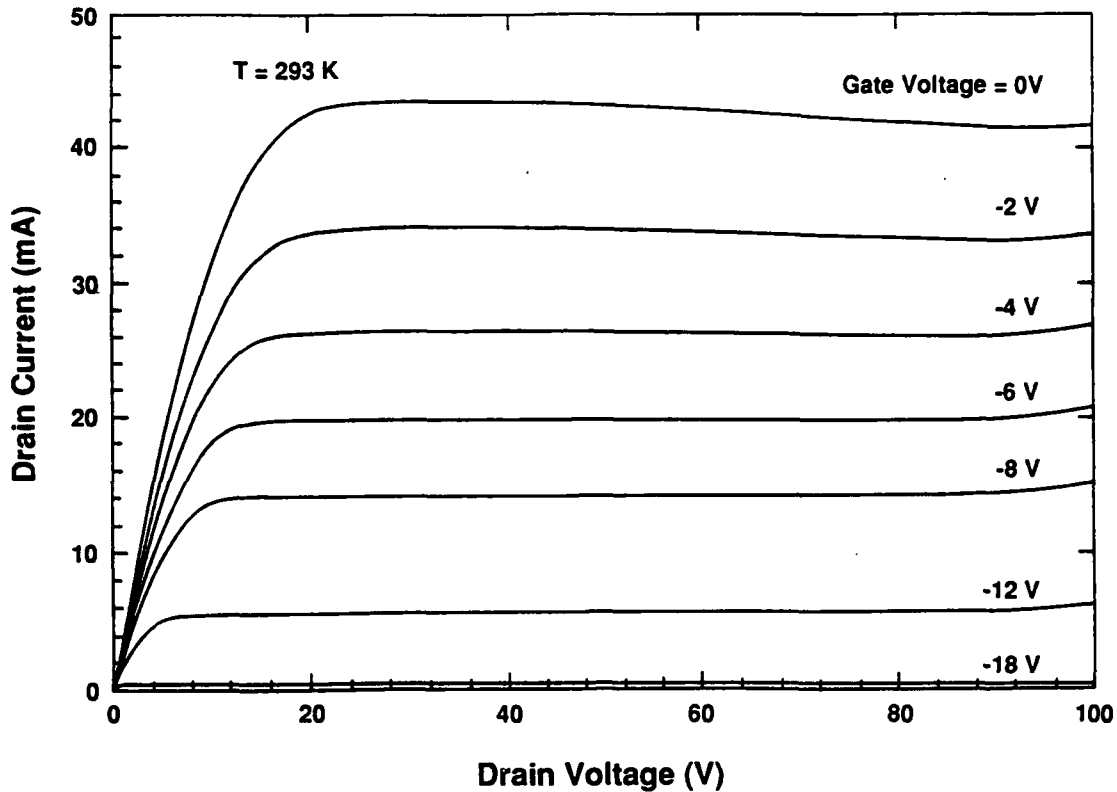


Figure 15: Drain current-voltage characteristics of a SiC MESFET demonstrating $V_d = 100$ V capability. Gate length and width are $24 \mu\text{m}$ and 1mm , respectively.

were also quite high compared to those shown in Figure 14, with power capability at a drain voltage of 100 V being in excess of 4 W per mm of gate width. The maximum transconductance was also higher, at 4.3 mS/mm. The subthreshold leakage current at $V_d = 100$ V and $V_g = -18$ V was $325 \mu\text{A}$. Since high field operation is desired for a SiC high frequency MESFET, these results were very promising. The remaining task is to translate this high field capability of the Schottky gate into a much smaller dimension gate length and a much smaller source-to-drain distance.

Devices with these smaller dimensions have been fabricated using the design illustrated in Figure 13. The n-type channels had a doping level of $n = 0.8\text{--}3 \times 10^{17} \text{ cm}^{-3}$ and a thickness of about $200\text{--}400$ nm, with buried p-layers ($p = 1\text{--}4 \times 10^{16} \text{ cm}^{-3}$) underneath. A typical I-V curve of one of these MESFETs is shown in Figure 16.

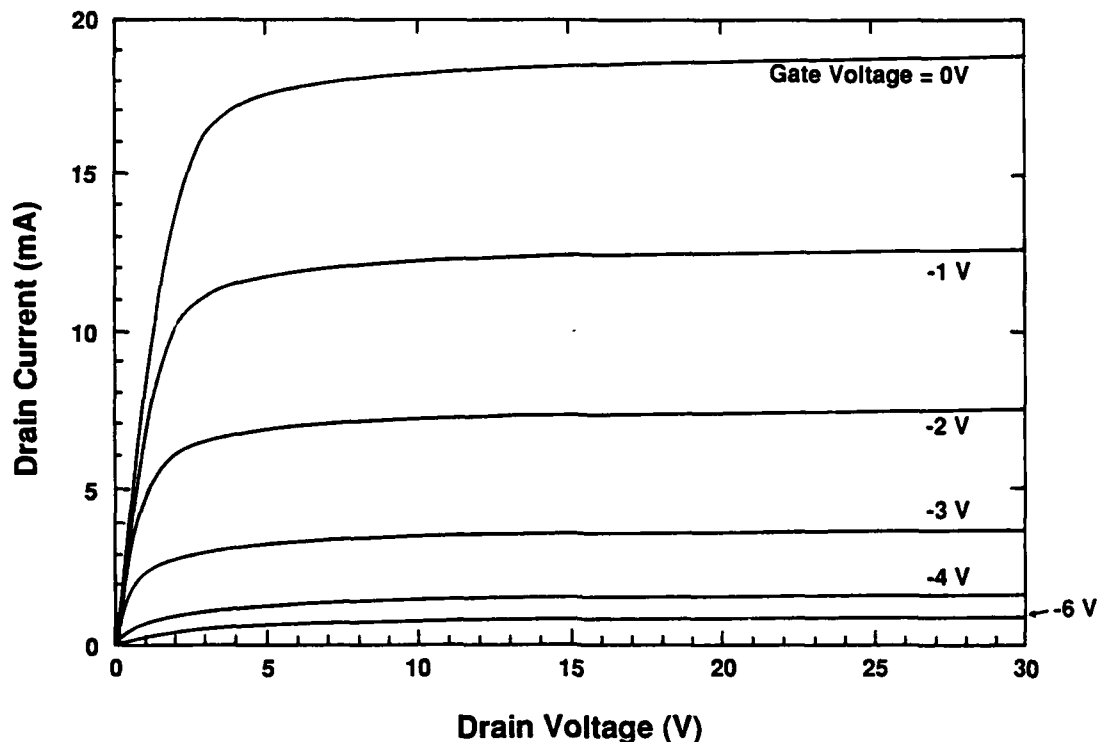


Figure 16: Drain current-voltage characteristics of a SiC MESFET using high power high frequency mask shown in Fig. 3. Gate length and width are $2\text{ }\mu\text{m}$ and 1 mm , respectively. Source-to drain distance is $4\text{ }\mu\text{m}$. The maximum transconductance is 6.4 mS/mm .

This particular device had a source-drain distance of $4\text{ }\mu\text{m}$ and a gate length of $2\text{ }\mu\text{m}$. The curve shows that a drain voltage of 30 V was obtained with a gate voltage of -6 V . The maximum transconductance of this device was 6.4 mS/mm and very stable current saturation was observed to $V_{DS} = 30\text{ V}$. This device was measured on at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 17 shows that this device has a threshold frequency (F_t) of 510 MHz , designated where the H21 parameter crosses 0 dB gain. The power gain (G_{max}) crosses 0 dB at about 380 MHz , indicating that F_{max} is at least 380 MHz .

A gain vs. frequency plot for a shorter gate length device is shown in Figure 18. This device had a gate length of $1.7\text{ }\mu\text{m}$ and had a correspondingly higher gain. The F_t of this device was 800 MHz and the F_{max} was at least 450 MHz . At 250 MHz the

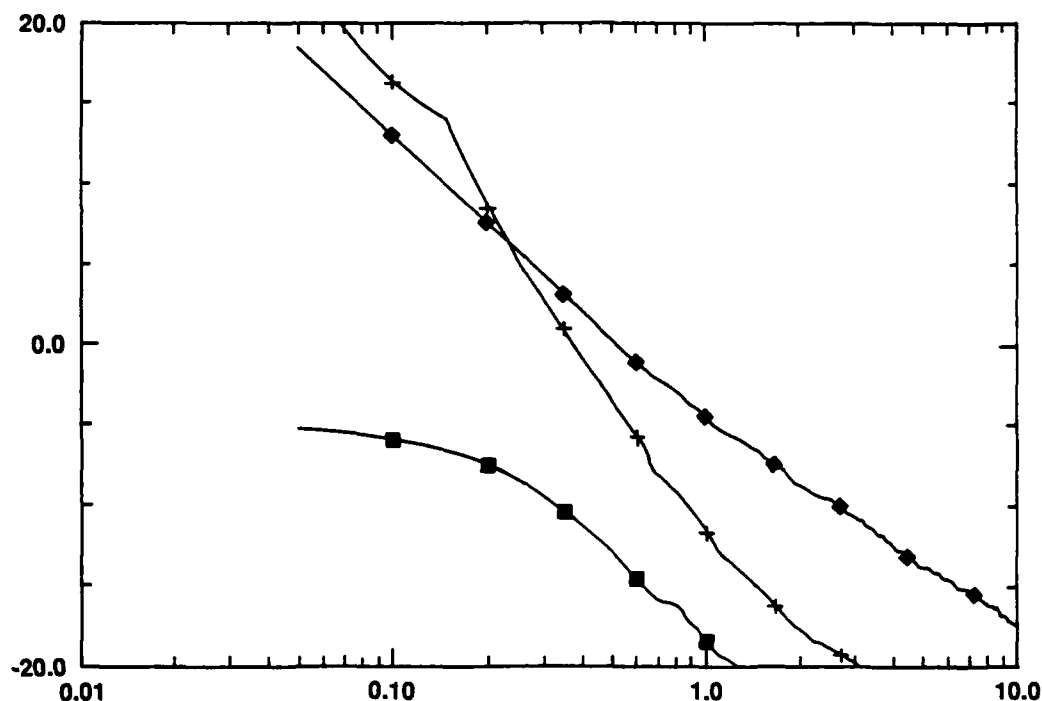


Figure 17: High frequency parameters, S_{21} , G_{\max} , and H_{21} , as a function of frequency for the $2\ \mu\text{m}$ gate length device shown in Fig. 9. Measurement conditions were $V_D = 30\ \text{V}$, $I_D = 14.2\ \text{mA}$, $V_G = -1.0\ \text{V}$, and $I_G = 1\ \mu\text{A}$.

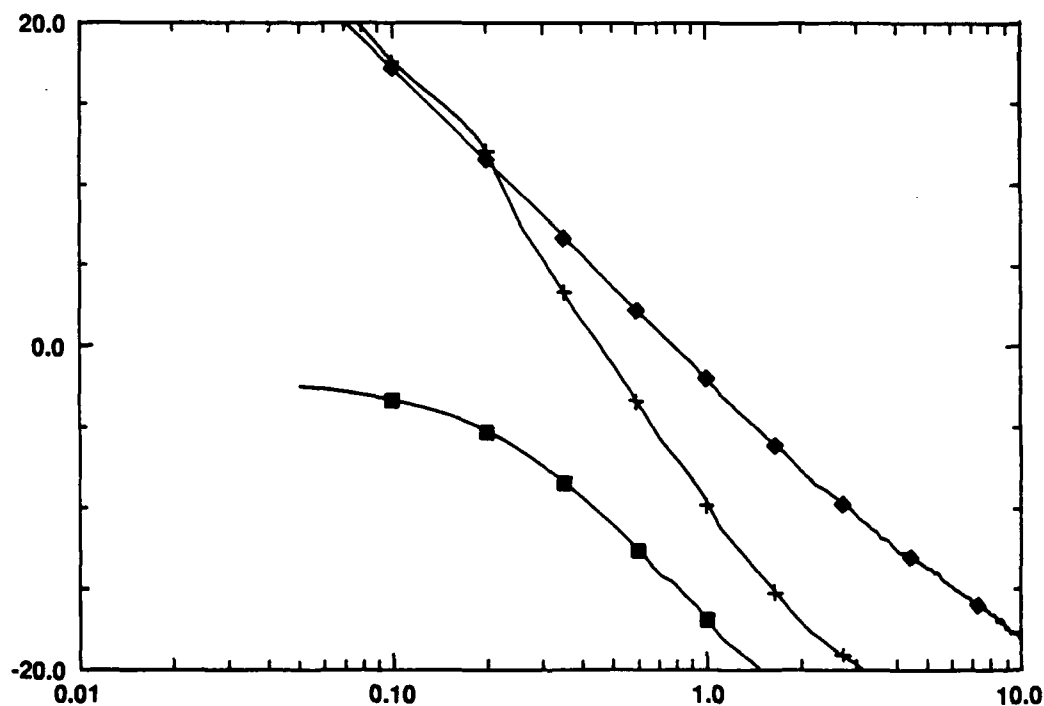


Figure 18: High frequency parameters, S_{21} , G_{\max} , and H_{21} , as a function of frequency for a $1.7\ \mu\text{m}$ gate length device. Measurement conditions were $V_D = 30\ \text{V}$, $I_D = 68.4\ \text{mA}$, $V_G = -1.0\ \text{V}$, and $I_G = 1.7\ \mu\text{A}$.

device had a current gain of 10 dB. While the high frequency gain always increased with decreasing gate length, as it should, the DC transconductance seemed to be virtually independent of gate length. For instance, the highest transconductance observed to date was 22 mS/mm for a 4 μm gate length device. Figure 19 shows a MESFET with a 2 μm gate length that had a relatively high transconductance of 12.3 mS/mm but still had a relatively short gate length. Although this device had a high on-current (>200 mA), it could not be cutoff because the channel was too thick. This device had the best high frequency gain of the devices measured, as shown in Figure 20. It had an F_t of 900 MHz and a F_{max} greater than 450 MHz.

The observed DC transconductances were quite low when compared to the long gate length device shown in Figure 15, considering the much smaller gate lengths and source-drain distances used in the high frequency design. This indicates that the limiting parasitic resistance is not related to mobility between the source and drain, but rather to contact resistance at the source and drain. It is apparent that the source and drain resistance are so dominant that the effect of reducing the gate length and source-drain spacing on the DC transconductance is negligible. The high frequency measurements show the effect of gate length because transit-time still plays a role, however, it is proposed that the overall high frequency gain of all of the devices was severely limited by the parasitic source and drain resistances. As such, the next iteration of 6H-SiC MESFETs was studied via modeling and subsequently fabricated with n^+ source and drain wells, as is common practice even for GaAs MESFETs.

The positive benefits of n^+ source and drain wells have been confirmed by modeling of similar 6H-SiC MESFETs at high frequency. The RF performance potential of 6H-SiC MESFETs at 0.5, 3, and 10 GHz was investigated. Making conservative assumptions for mobility and contact resistance values, 240 $\text{cm}^2/\text{V}\cdot\text{sec}$ and $1 \times 10^{-4} \Omega\cdot\text{cm}^2$ respectively, and assuming n^+ source and drain wells, maximum power was calculated for each of these frequencies. The assumed dimensions of the device were a 1 μm gate length, a 1 μm source-gate distance, and a 2 μm gate-drain

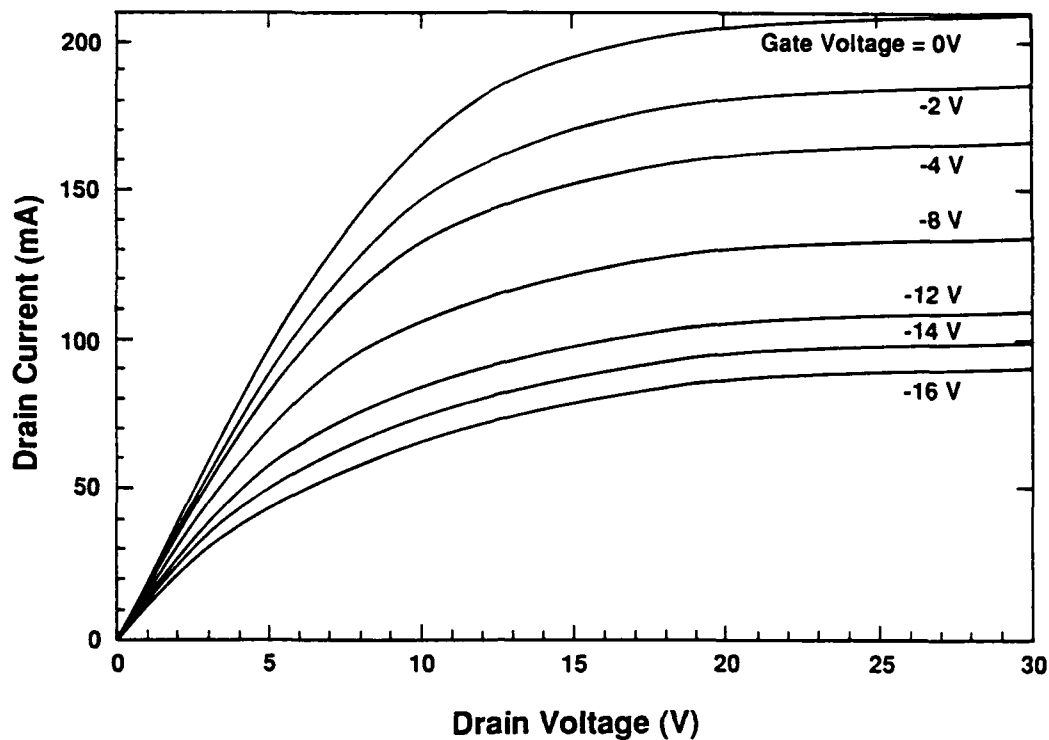


Figure 19: Drain current-voltage characteristics of a SiC MESFET. Gate length and width are $2\ \mu\text{m}$ and $1\ \text{mm}$, respectively. Source-to drain distance is $4\ \mu\text{m}$. The maximum transconductance is $12.3\ \text{mS/mm}$.

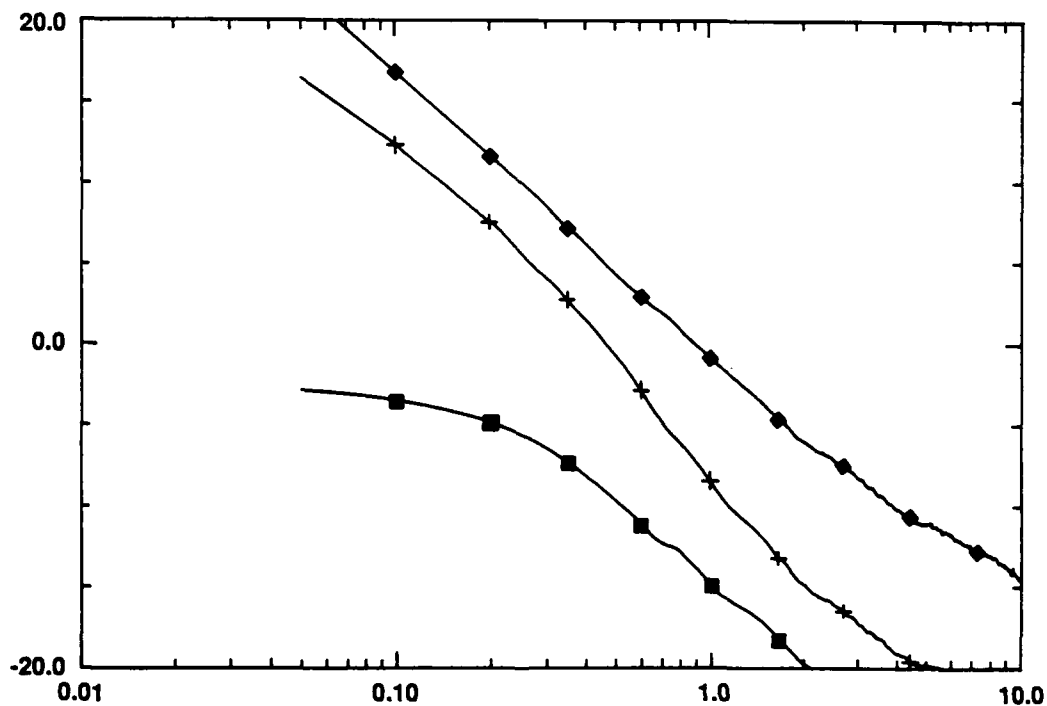


Figure 20: High frequency parameters, S_{21} , G_{max} , and H_{21} , as a function of frequency for the $2\ \mu\text{m}$ gate length device shown in Figure 19. Measurement conditions were $V_D = 30\ \text{V}$, $I_D = 189\ \text{mA}$, $V_G = -1.0\ \text{V}$, and $I_G = 1\ \mu\text{A}$.

distance. The 6H-SiC devices produced about 630 W, 158 W and 45 W at those three frequencies, respectively. This corresponds to a normalized RF output power of about 2.5 W/mm of gate length. This value compares quite favorably with the 0.5-0.6 W/mm obtained with GaAs power FETs. Power-added efficiency and gain were also quite good and are shown, along with output power, as a function of frequency in Figure 21. All devices were biased for class A operation and CW conditions were assumed. Increased output power could be obtained from class B or C operation and/or pulse bias conditions; however, these modes of operation were beyond the scope of this investigation. Due to the excellent thermal conductivity of SiC, thermal modeling of the MESFETs showed that they are not thermally limited and should, in fact, be operable at elevated temperatures.

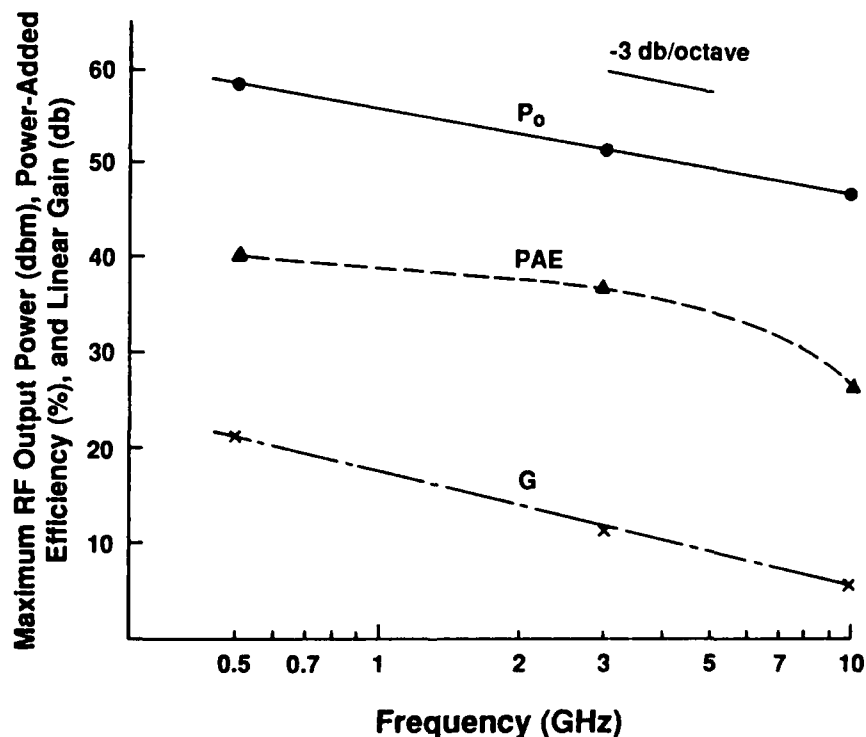


Figure 21: Modeled maximum RF performance as a function of frequency for 6HSiC MESFETs ($V_{DS} = 40$ V, $I_{DS} = I_{DSS}/2$, $L_g = 1$ μ m). RF output powers of 630 W, 158 W, and 45 W were obtained at 0.5, 3, and 10 GHz, respectively.

The DC transconductances observed for the devices discussed above were quite low when compared to other long gate length MESFET devices fabricated at Cree, considering the much smaller gate lengths and source-drain distances used in the high frequency design. This indicated that the limiting parasitic resistance is not related to mobility between the source and drain, but rather to contact resistance at the source and drain. It was apparent that the source and drain resistance are so dominant that the effect of reducing the gate length and source-drain spacing on the DC transconductance was negligible. The device modeling described above further proved this to be true. The modeled channel resistances were in the range of 35 Ω , while the measured resistances were more in the range of 110 - 130 Ω . Thus, as noted above the next iteration of 6H-SiC MESFETs was fabricated with n^+ source and drain wells, as was discussed in the previous section. This not only greatly reduced the resistivity of the SiC, but also greatly reduced the contact resistance of the ohmic contacts. The measured channel resistance of the devices with the n^+ source and drain wells were very close to the modeled resistances having values ranging from 30 - 37 Ω .

A typical DC current-voltage plot of one of these 6H-SiC MESFETs with an n^+ source and drain is shown in Figure 22. This device had a gate length and width of 1.8 μm and 1 mm, respectively. Drain voltages of 20 V were achieved with relatively good current saturation; higher drain voltages resulted in a detrimental increase in source/drain leakage current. These characteristics show a very good match with the modeling for a 1.8 μm device up to $V_D = 10$ V, where the effects of source/drain leakage current and gate leakage current begin to show. This match is very encouraging, indicating that the modeling for the optimal devices that was performed should be quite accurate. The DC power output of this device was about 5 W/mm of gate width. The maximum transconductance of this device was 17 mS/mm at $V_D = 20$ V and $V_G = 0$ V, and the measured channel resistance was 33.4 Ω . The gate leakage current at $V_D = 20$ V and $V_G = -15$ V was 1-2 mA, which is much larger than gate

leakage currents observed in previous MESFET devices. This increased leakage current, as well as increased source-drain leakage current, is thought to be due to the sample having a higher defect density than wafers that were used previously.

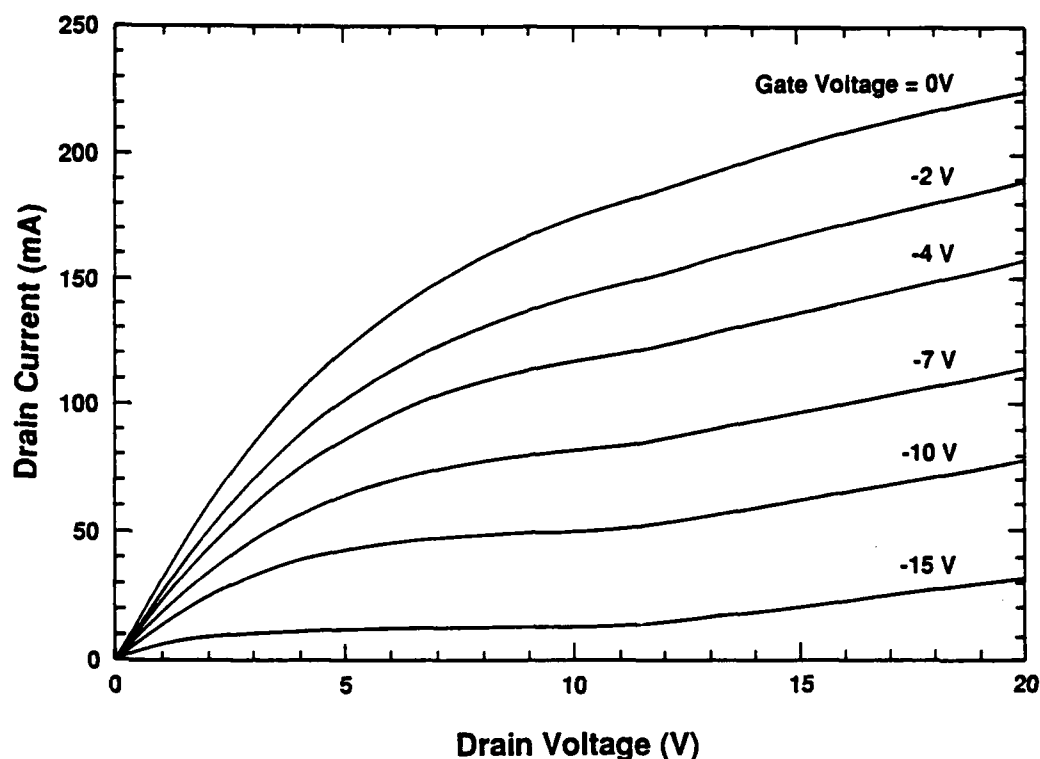


Figure 22: Drain current-voltage characteristics of a SiC MESFET using high power high frequency mask. Gate length and width are $1.8\text{ }\mu\text{m}$ and 1 mm , respectively. Source-drain distance is $4\text{ }\mu\text{m}$. The maximum transconductance is 17 mS/mm .

The positive benefits of n^+ source and drain wells were also confirmed by measurement of the 6H-SiC MESFETs at high frequency. This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 23 shows that this device has a threshold frequency (F_t) of 1.35 GHz , designated where the H_{21} parameter crosses 0 dB gain. The device has an F_{max} of 500 MHz , where the power gain (G_{max}) crosses 0 dB gain. The previously observed average values for F_t and F_{max} were 600 MHz and 380 MHz , respectively.

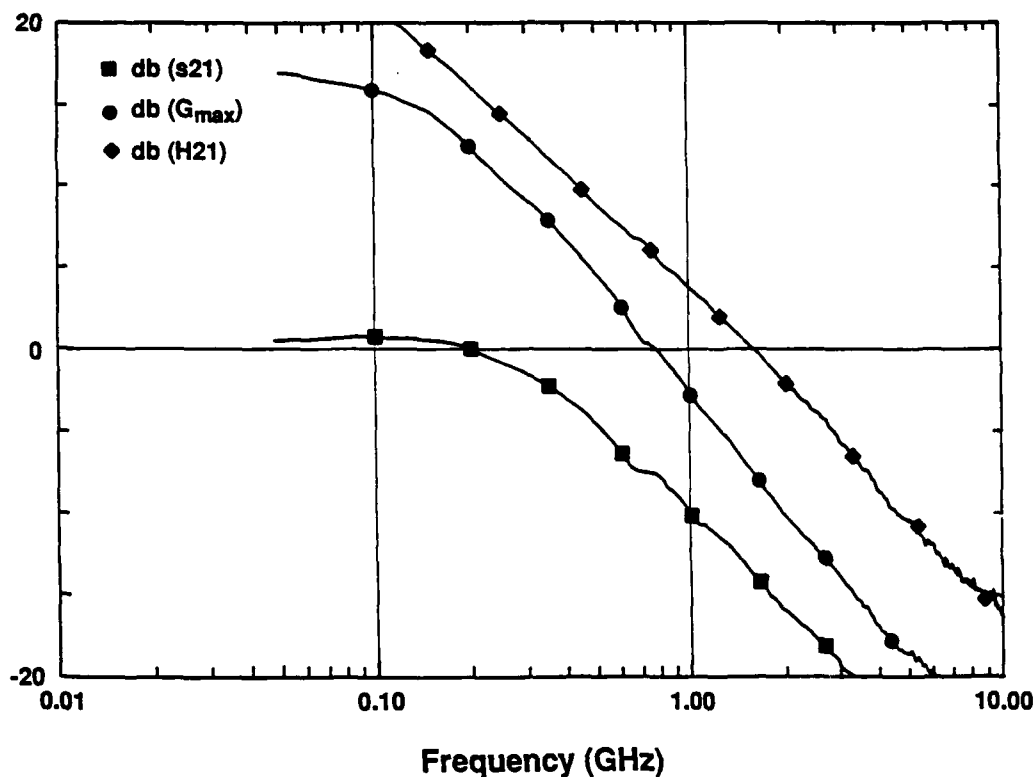


Figure 23: High frequency parameters, S21, G_{\max} , and H21, as a function of frequency for the 1.8 μm gate length device shown in Figure 22. Measurement conditions were $V_D = 20\text{ V}$, $I_D = 252\text{ mA}$, $V_G = 0\text{ V}$, and $I_G = 142\text{ }\mu\text{A}$.

While the DC characteristics of this device were very close to the modeled characteristics, the high frequency measurements were not. The modeling for the 1.8 μm gate length showed that the device should have had an 11 dB gain at 3 GHz (see section on MESFET modeling). Obviously, there was still a very large parasitic present in the device that greatly reduced the high frequency gain. Initially, it was thought that the "killer" parasitic was the gate capacitance due to the gate contact pad. The total gate capacitance measured was 5.75 pF. Of this capacitance, only about 1.7 pF was due to the area of the Schottky gate contact, with the other 4 pF arising from the 300 nm thick Si_3N_4 isolation pad. Thus the gate capacitance was 3.4 times higher than the modeling assumed. However, when the modeling calculations were performed with this higher gate capacitance, the high frequency performance was not degraded enough to account for the measured high frequency parameters.

The next parasitic that was addressed was the gate resistance. The gates of these devices were very thin (100 nm). Given this very small cross-section and the long finger length (500 μm), the series resistance along the gate fingers was very high, with values in the range of 150 -300 Ω . When the modeling was performed using this high gate resistance, the high frequency gain was severely degraded to values that were very close to those that were measured. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω . These low values of gate resistance are achieved by using thick overlayers of gold (which has a very low resistivity) on top of the gate contacts. As such, future 6H-SiC MESFETs will be fabricated using gold overlayers on the gate contact.

In order to confirm the effects of gate resistance on the high frequency parameters, an overlayer was deposited on top of the gate contact of the same device shown in Figures 22 and 23. Since gold was not available at the time, and it was not certain that a thick layer could be "lifted off," a 200 nm thick overlayer of Al was deposited instead. While far from optimal, a significant reduction in gate resistance did result from this overlayer. This overlayer actually caused an unexpected noticeable improvement in the DC characteristics of the device. The I-V characteristics shown in Figure 24 show that the current saturation was slightly improved and the maximum transconductance increased from 17 mS/mm to 18 mS/mm. A gain vs. frequency plot for the same device with the Al overlayer is shown in Figure 25. The F_{max} of this device showed a marked increase from 500 MHz to 770 MHz, and the F_t increased from 1.35 GHz to 1.6 GHz. At 500 MHz, the device had a power gain of 4.6 dB and a current gain of 8.5 dB. Based on these results, it is apparent that the gate resistance is by far the most important parasitic to be addressed. When this problem is minimized, the gate capacitance will be addressed as the major parasitic.

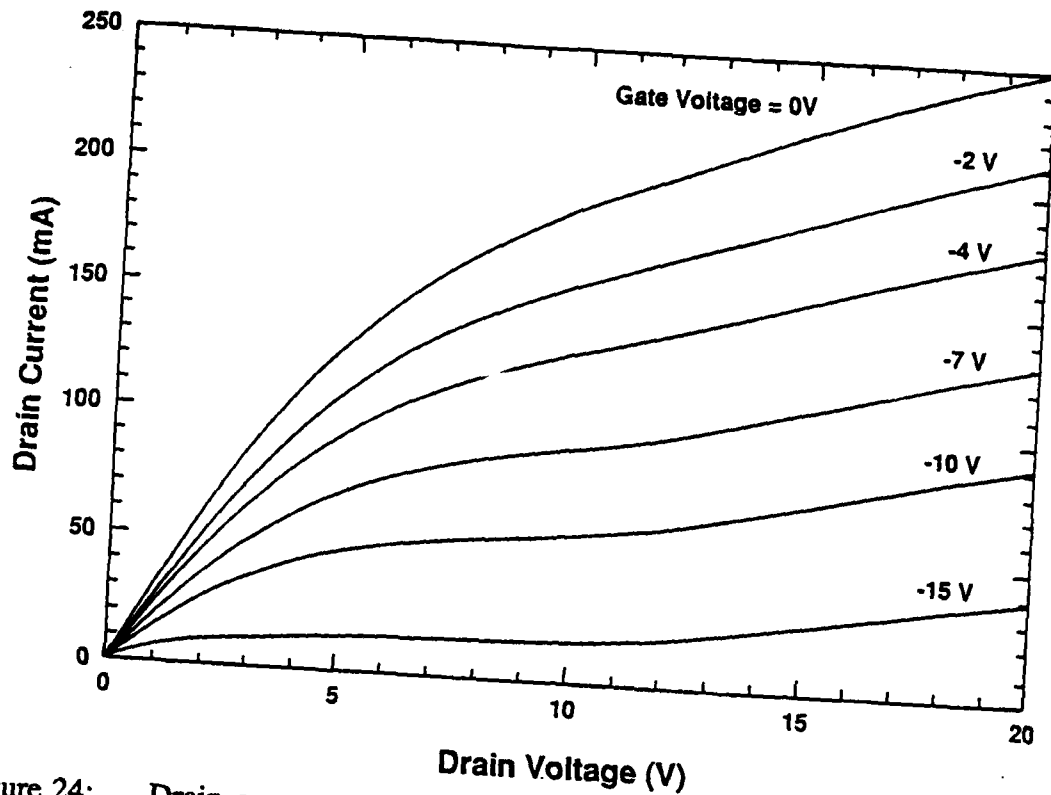


Figure 24: Drain current-voltage characteristics of the same SiC MESFET shown in Figures 22 and 23 after deposition of a 200 nm thick Al overlayer on the gate. The maximum transconductance is 18 mS/mm.

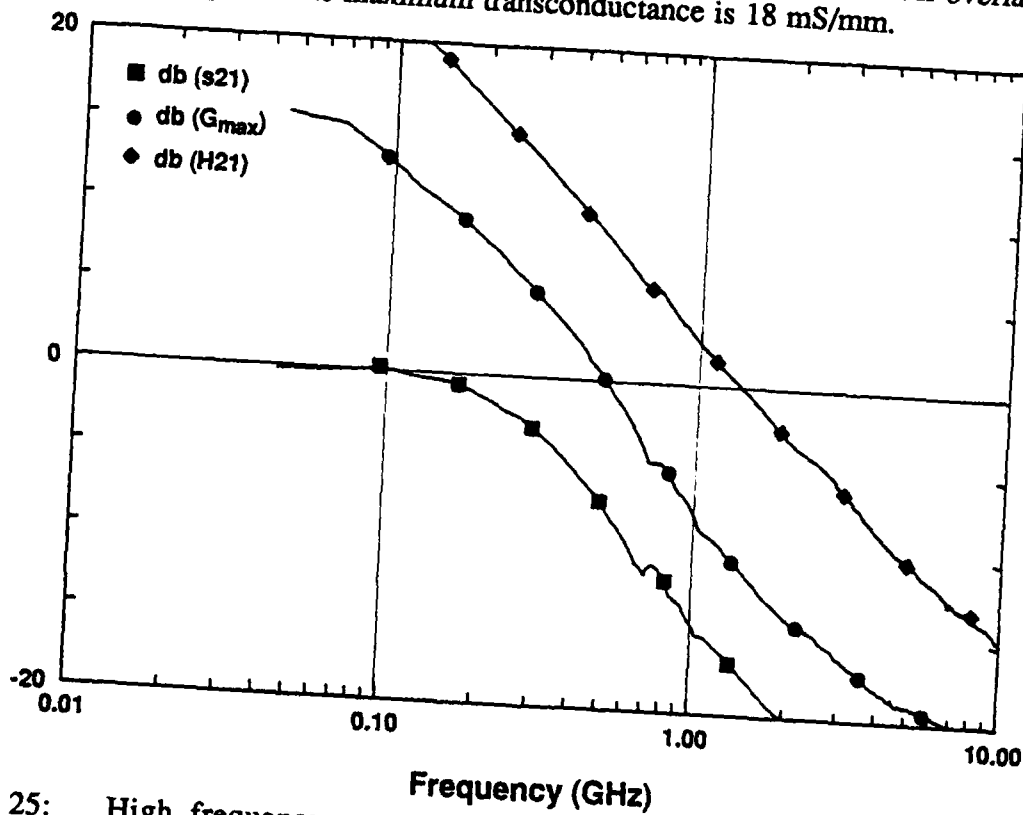


Figure 25: High frequency parameters, S_{21} , G_{max} , and H_{21} , as a function of frequency for the device in Fig. 6 with the Al gate overlayer. Measurement conditions were $V_D = 20$ V, $I_D = 240$ mA, $V_G = 0$ V, and $I_G = 123$ μ A.

These results are very promising in several respects. Even with the relatively long $1.8\text{ }\mu\text{m}$ gate length and the very degrading parasitic gate resistance, 6H-SiC MESFETs were fabricated that had very good UHF characteristics, particularly considering the high power per unit gate width observed. Secondly, it appears that the MESFET modeling is quite accurate, meaning that 6H-SiC should allow very high power devices rated at frequencies up to 10 GHz to be fabricated. The major issues now are to minimize the same parasitics that have to be dealt with in any high frequency device in any material, primarily gate resistance and gate capacitance, and to further reduce the gate length for higher gain.

In order to further improve both the device design and the fabrication procedures for 6H-SiC MESFETs, a new mask set has been designed. This new design, shown in Figure 26, is still a 1 mm gate width device consisting of two $500\text{ }\mu\text{m}$ long gate fingers, but it uses much smaller source and drain ohmic contact areas that make the overall device size 27% smaller. The smaller contact area is allowed because of the n^+ source and drain to be used, as opposed to the previous design. Shorter gate lengths are used on this mask, varying from $0.6\text{ }\mu\text{m}$ to $1.0\text{ }\mu\text{m}$, although it is expected that these lines will spread during processing, resulting in actual gate lengths ranging from $0.8\text{ }\mu\text{m}$ to $1.3\text{ }\mu\text{m}$. The gate - drain spacing has been increased from $1\text{ }\mu\text{m}$ to $1.5\text{ }\mu\text{m}$ to allow higher drain voltages to be attained. The source - gate spacing is $1\text{ }\mu\text{m}$ (accounting for gate line spread) for all of the devices except the smallest gate length, which has a $0.5\text{ }\mu\text{m}$ spacing. To further reduce the gate capacitance, the gate contact pad area has been reduced to the minimum value that still allows reliable wire bonding. Finally, source and drain metal overlayers are used to facilitate better contacting for probing as well as wire bonding.

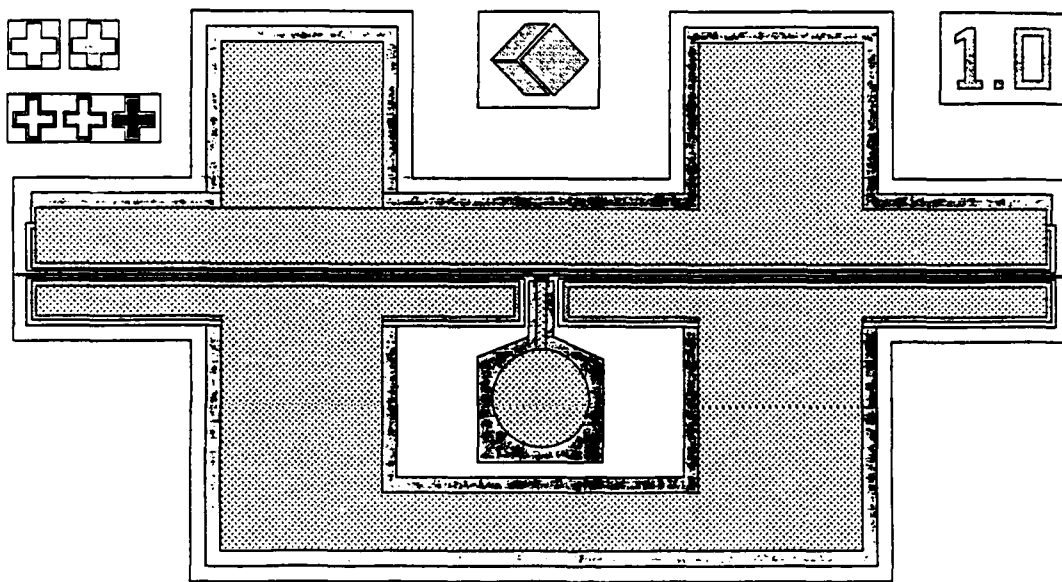


Figure 26: New design for high power, high frequency SiC MESFET. Gate lengths vary from $1.0\text{ }\mu\text{m}$ to $0.6\text{ }\mu\text{m}$, and source-to-drain distances vary from $3.5\text{ }\mu\text{m}$ to $2.9\text{ }\mu\text{m}$. The gate width is 1 mm .

p-n Junction Diode Design, Fabrication and Characterization. Alpha (6H)SiC pn junction diodes have been fabricated that demonstrate very good avalanche breakdown characteristics at very high voltages, as shown in Figure 27. Because of these results, further IMPATT structures were based on pn junction diodes. The initial design for SiC IMPATTs used a mesa pn junction structure with a passivated sidewall. A variety of epilayer structures were grown so that the best configuration could be determined. Both p+-n and n+-p flat profiles were grown, as well as the p+-n+-n- high-low structure discussed above. The epilayers were all grown on n+ substrates for maximum conductivity, and then mesas were reactive ion etched in the SiC to a depth of $14\text{ }\mu\text{m}$. The sidewalls were passivated via thermal oxidation, and the p-type ohmic contacts were defined and annealed on top of the mesas.

The original processing scheme was to then lap away the substrate from the backside until only the mesas were left. Ohmic contacts would then be deposited on the backside of these dots, and the individual mesas, or diodes would subsequently be

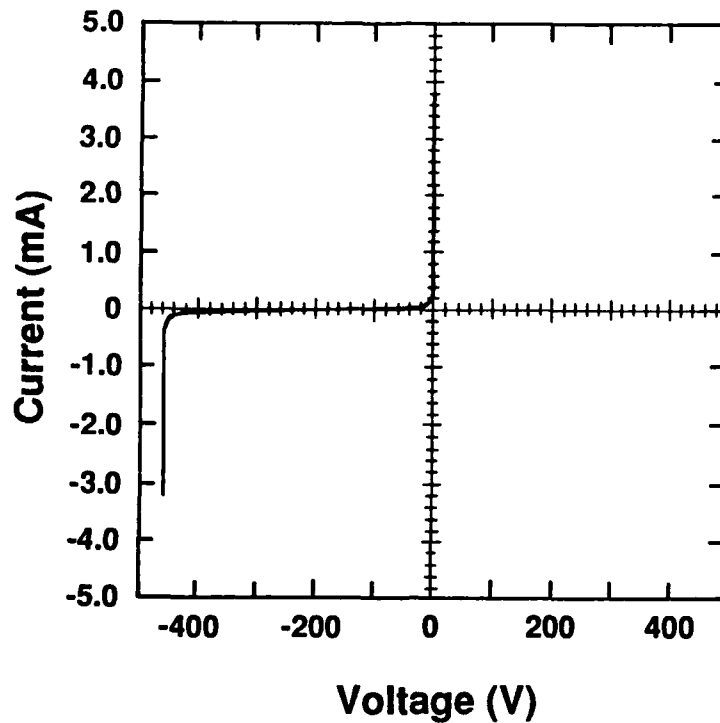


Figure 27: Current-voltage characteristics of a 6H-SiC pn junction diode, showing avalanche breakdown at 400 V.

annealed. This would result in very small discrete diode "dots" that are 14 μm thick. However, after much experimentation it was determined that this process was difficult to perform and was not a promising technique. It is planned to finish these devices instead by lapping the wafer to a thickness of about 60-70 μm , and then depositing and patterning Al on the backside to allow reactive ion etching of contact via holes to a depth of about 40 μm . After the Al mask is stripped, the Ni ohmic contact can be deposited over the entire backside, and the wafer can be annealed. This scenario would allow the devices to be handled in wafer form instead of trying to handle very small discrete dots, but would still allow the effective substrate thickness to be very thin.

IV. Interfacial Studies of Metal Contacts to Alpha (6H)-SiC

A. Overview

For an ideal, abrupt junction the barrier height is defined by the Schottky-Mott limit, or the difference between the metal workfunction and the electron affinity of the

semiconductor. However, interface states and chemical reactions between the metal and semiconductor cause deviations from ideality. In fact, Pelletier *et al*[2] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states. In effect, this result indicates little dependence of barrier height on the work function of the metal, which has often been the case in practice. On the other hand, Waldrop *et al*[3] have reported strong work function dependence for metal/ β -SiC barrier heights, giving encouragement for the ability to control electrical characteristics on 6H-SiC. The α polytype, 6H-SiC, has been chosen for this study due to the ability to grow bulk crystals and thin films which have low defect densities[4].

Both temperature and technique for cleaning the SiC (0001) surface will be critical parameters in this study. Stability of the contacts at high temperature (500°C range) is important since this wide bandgap semiconductor possesses properties which make it attractive for high temperature applications. Surface cleaning techniques, e.g. ex-situ RCA clean and buffered oxide etch (BOE) and in-situ remote hydrogen plasma, will be compared in terms of their effect on surface chemistry and microstructure.

Six metals have been chosen for this study based on their work functions and phase diagrams with Si and C; these include Pt and Se for rectifying contacts and Ti, Hf, Sr, and Co for potential ohmic contacts. These metals were chosen based on the theory that metals with high work functions should form good rectifying contacts to n-type SiC, while metals with low work functions are desired for ohmic contacts. Microstructural information will be obtained from low energy electron diffraction (LEED) and high resolution transmission electron microscopy (HRTEM). Auger electron spectroscopy (AES) and x-ray photoelectron spectroscopy (XPS) will give chemical information about the surfaces and interfaces. This chemical and microstructural information will be correlated with electrical characteristics obtained from I-V measurements. Preliminary studies have been performed for both Se and Ti on 6H-SiC and will be described in detail in this report.

B. Experimental Procedure

The substrates used in this study are 6H-SiC wafers provided by Cree Research, Inc. The wafers are 1" in diameter and are nitrogen doped n-type ($\sim 5 \times 10^{17}/\text{cm}^3$). The surfaces were Si-terminated, referred to as (0001).

Selenium deposition was performed by Frank Jansen at Xerox Corporation in Webster, New York. Prior to deposition the substrates were cleaned by a conventional RCA clean: 10 min. in (5:1:1) $\text{H}_2\text{O} / \text{H}_2\text{O}_2 / \text{NH}_4\text{OH}$, 5 min. water rinse, 10 min. in (5:1:1) $\text{H}_2\text{O} / \text{H}_2\text{O}_2 / \text{HCl}$, and an additional 5 min. water rinse. Subsequently, the substrates were etched in 10:1 BOE to remove any oxide. A 200 nm amorphous layer of selenium was thermally evaporated onto substrates patterned with photoresist. A contact diode pattern was subsequently achieved by "lift'off" in acetone.

Current-voltage measurements of the selenium film were analyzed with an HP 4145A Semiconductor Parameter Analyzer. A mercury arc lamp with 150 W maximum power was used to illuminate the sample.

Titanium was thermally evaporated at room temperature from a hot wire filament at a rate of approximately 0.2 A/s. The pressure in the chamber was in the 10^{-9} Torr range. The SiC substrates were cleaned ex-situ by an RCA clean and then spun with (10:1:1) $\text{H}_2\text{O} / \text{HF} / \text{ethanol}$. Two sets of experiments were performed. In the first set of experiments, 200 Å of Ti was deposited in steps of 50 Å. The sample was then annealed to 900°C in 100°C steps for 10 min. at each temperature. The sample was analyzed in-situ by retarding LEED/ Auger both before deposition and after each deposition / anneal. Approximately 200 Å of Ti was deposited on a second substrate. Again, LEED and Auger analyses were performed, but the sample was not annealed. SEM photographs were taken ex-situ of both the annealed and non-annealed samples to reveal surface topography.

C. Results

Current-voltage measurements indicated that the selenium contacts were non-conductive under ambient lighting conditions. Due to its photoconductive nature, measurements were taken while the sample was illuminated with a 150 W mercury arc lamp. Although optimum lighting conditions were not obtained with this set-up, the conductivity of the Se film increased as the light intensity reaching the sample increased.

LEED patterns taken of the 'clean' SiC surfaces before Ti deposition showed a bulk $\sqrt{3} \times \sqrt{3}$ pattern, indicative of no surface reconstruction. After depositing 50 Å of Ti, the LEED pattern did not change, as was the case after depositing 200 Å (Figure 28). The sample was then annealed to 900°C. After each anneal, the LEED pattern remained identical to the LEED pattern obtained for the SiC substrate.

In conjunction with the structural information obtained from LEED, AES measurements were taken as a means of fingerprinting elements in the near-surface region. Figure 29 shows a series of Auger spectra taken both before and after depositing Ti. The amount of oxygen on the surface was below the detection limits of the system. After depositing 50 Å of Ti (no anneal), the Si and C peaks disappeared, and 2 peaks characteristic of Ti appeared. A total thickness of 200 Å was deposited. After annealing to 500°C or 600°C, the Si and C peaks began to reappear. An interesting result occurred at 800°C; a sharp Si peak appeared, while a smaller carbon peak remained.

SEM pictures were taken of both the annealed and non-annealed Ti films. Figure 30 shows a smooth topography for the non-annealed film. Faint, randomly oriented striations appeared to be present at lower magnifications, probably due to surface roughness of the SiC left after polishing. The surface topography after annealing to 900°C (Figure 31) is no longer smooth; instead, the surface appears dimpled, but still uniform.

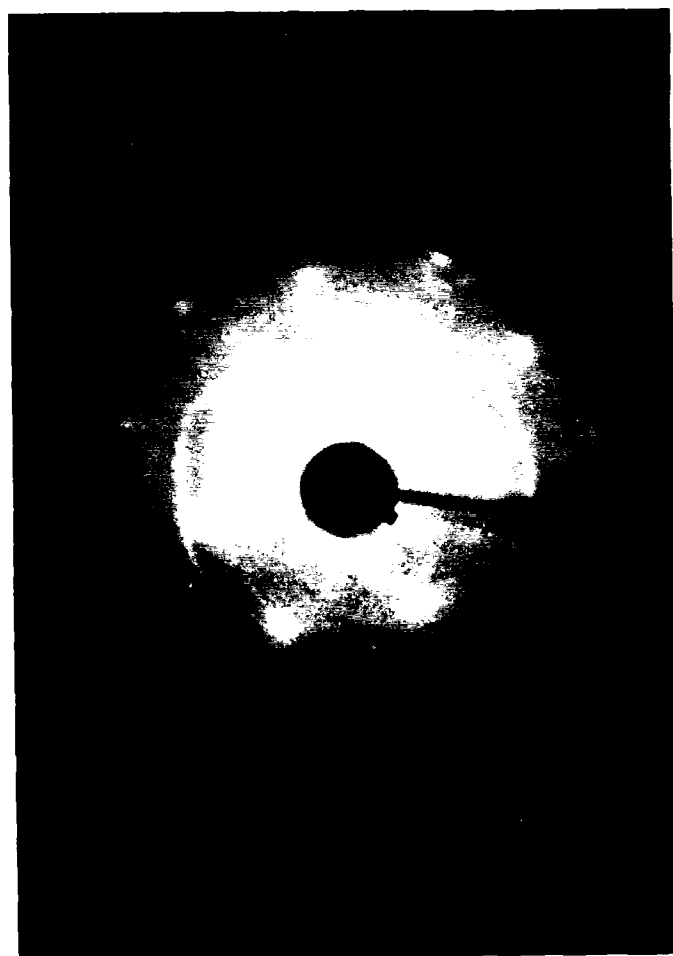


Figure 28. LEED pattern of 200 Å Ti film (n0 anneal) on 6H-SiC(0001).

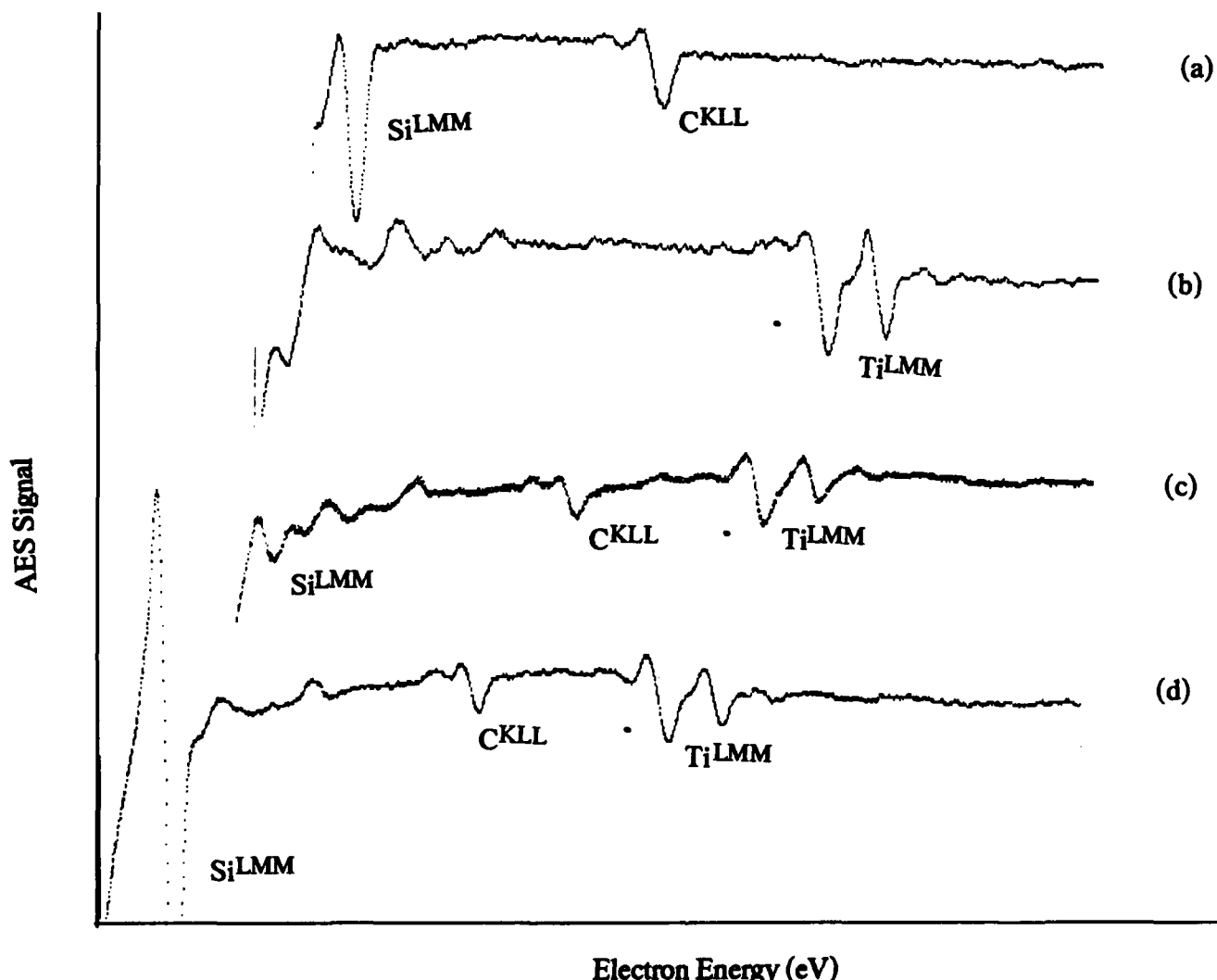


Figure 29. AES spectra of (a) 6H-SiC (0001) surface, (b) 200 Å Ti on SiC (as-deposited at room temp.), (c) 200 Å Ti on SiC (annealed to 600°C), and (d) 200 Å Ti on SiC (annealed to 800°C).

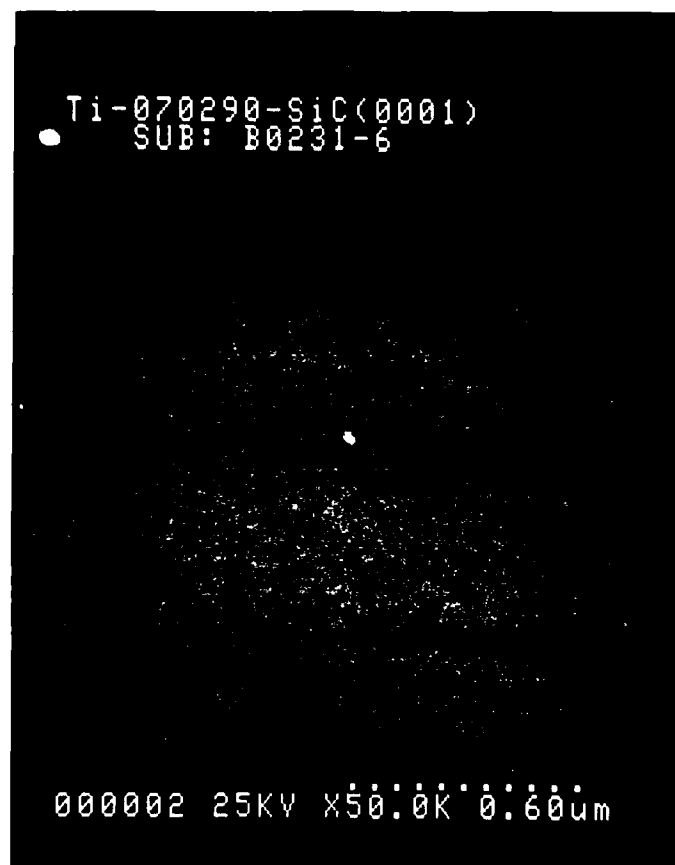


Figure 30. SEM picture of 200 Å Ti film (as-deposited at rm. temp.) on 6H-SiC (0001). (Magn. = 50K).

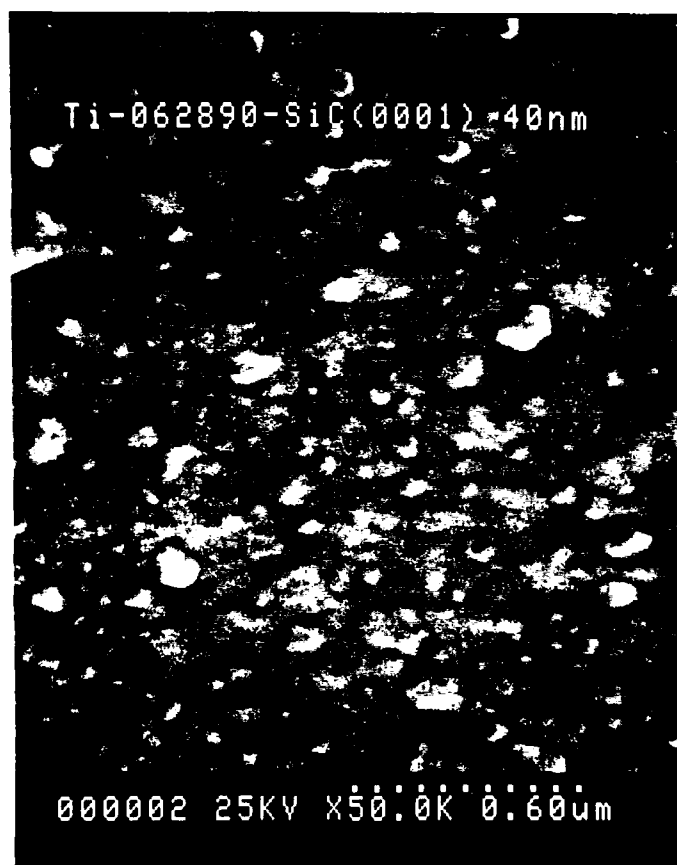


Figure 31. SEM picture of 200 Å Ti film (annealed to 900°C) on 6H-SiC (0001). (Magn. = 50K).

D. Discussion

Because selenium has a low electron drift mobility ($4 - 8 \times 10^{-3} \text{ cm}^2/\text{V-s}$) and high trap densities (10^{19} cm^{-3} at 0.28 eV for electrons and 10^{21} cm^{-3} at 0.14 eV for holes)[5], high intensity illumination will be necessary to yield good conductive properties. Therefore, 1000 W tungsten-halogen bulbs have been purchased to optimize illumination conditions. If electrons are promoted into the conduction band from the valence band, the selenium will act like a metal; if electrons are promoted from states within the bandgap, the selenium will act as an intrinsic semiconductor.

The LEED patterns indicate that the titanium films have the same crystal structure as the silicon carbide substrates. This result is not surprising after comparing the crystal structures of each of the materials separately. The substrates have a hexagonal crystal structure with lattice parameter $a = 3.08 \text{ \AA}$ [6]. The crystal structure of Ti is also hexagonal with $a = 2.95 \text{ \AA}$ [7]. This difference in lattice parameters corresponds to only a 4% lattice mismatch. Similar results are predicted for hafnium, its crystal structure (hexagonal, $a = 3.19 \text{ \AA}$)⁶ corresponding to less than 4% mismatch with 6H-SiC.

Clues to the chemistry at the interface between Ti and SiC are given by the Auger spectra (Figure 29) and by the work of Bellina *et al*[8], who suggest the formation of TiC at Ti/SiC interfaces and diffusion of Si to the surface. The spectrum taken after annealing at 800°C shows that the surface is Si-rich and contains a modest amount of carbon. However, in order to positively identify and carbide and/or silicide formation, analysis by XPS and Raman spectroscopy will be performed.

The combination of the Auger spectra and the SEM pictures give evidence to 2-dimensional growth of the Ti film. The Auger spectrum taken after depositing 50 Å of Ti did not contain any Si or C peaks, indicating complete coverage of the SiC surface with Ti. The topography shown in Figure 30 shows a smooth surface absent of islands, islands being indicative of 3-dimensional growth. The dimpled surface (Figure

31) resulting from annealing to 900°C suggests that formation of a carbide or silicide at the interface has extended throughout the thickness of the Ti film.

E. Conclusions

Six metals have been chosen as contacts to 6H-SiC for this study. In order of decreasing work function, this list includes Se, Pt, Co, Ti, Hf, and Sr. It is hoped that by carefully preparing the SiC surface, the Fermi level will be unpinned, thereby giving better control of electrical characteristics at the contact.

Amorphous selenium has been deposited, and preliminary electrical measurements have been taken. These measurements, along with the known photoconductive behavior of Se, suggest that high intensity illumination will be necessary to measure electrical characteristics of the contacts. Tungsten-halogen bulbs (1000 W) have been purchased for this purpose.

Titanium has been deposited at room temperature onto SiC wafers, which were RCA cleaned and spun with H₂O / HF / ethanol. LEED patterns for the SiC substrate and the Ti film were the same, indicating identical crystal structures. The Auger spectra and SEM pictures taken of a sample which had not been annealed indicate a 2-dimensional growth process of the Ti crystal. Auger spectra taken after annealing to 900°C show a Si-rich surface with some C also present. More interfacial studies using XPS and Raman spectroscopy should identify carbide and/or silicide formation.

V. Characterization of Schottky Contacts on Alpha (6H)-Si (Palmour-Cree Research, Inc.)

A. Overview

As discussed above, at present the most promising device for microwave performance of SiC is a MESFET. If a high voltage SiC MESFET is to be fabricated, the first requirement is to have a high voltage Schottky contact; the second requirement is that this Schottky contact must operate reliably at elevated temperatures because of the high power levels anticipated for these devices. While

Au Schottky contacts have been shown to be quite good for both β -SiC[9,10] and 6H-SiC at room temperature, they have also been shown to degrade rapidly with elevated temperatures[10], in the range of 300°C. Therefore, a more stable Schottky contact is required for a high power microwave device. Viability of this contact in a high voltage MESFET must then be proven, and finally a high power microwave device can be designed and fabricated.

Both platinum and gold contacts were deposited on n-type epilayers on n-type SiC substrates and characterized. The gold acted as a "control" contact for the platinum experiments, because gold Schottky contacts on SiC have been previously characterized[9,10]. While providing very good rectifying characteristics at room temperature, the gold contacts permanently degraded when heated above 300°C, as was noted in the previous studies[10]. Conversely, the platinum Schottky contacts demonstrated very good rectifying characteristics in both the as-deposited condition and after annealing at a variety of temperatures.

Different n-type concentrations were investigated for use as the conducting channel of a MESFET, with the emphasis on the effect carrier concentration had on the leakage current and the breakdown voltage of the Schottky diode. The Pt Schottky contacts on n-type SiC with $n = 4 \times 10^{16} \text{ cm}^{-3}$ generally experienced breakdown at a reverse bias of -85 V to -92 V. This corresponds to a maximum field strength greater than $6 \times 10^5 \text{ V/cm}$, which is higher than Si or GaAs can even theoretically achieve. For an annealed Pt Schottky on a sample with $n = 6 \times 10^{16} \text{ cm}^{-3}$, breakdown occurred at -70 V reverse bias and the leakage current remained quite low ($<1 \mu\text{A}$) at voltages below this, as shown in Figure 32. Samples were also measured on films with $n = 1 \times 10^{17} \text{ cm}^{-3}$ and $n = 3.3 \times 10^{17} \text{ cm}^{-3}$, the latter of which is shown in Figure 33. This shows that for reverse biases less than -30 V, films doped as high as $3.3 \times 10^{17} \text{ cm}^{-3}$ could be used for MESFETs, which should allow very high transconductances (very low resistive losses). Even with this high doping level the Schottky did not truly breakdown until a reverse bias of -46 V was reached. Even

more encouraging was the fact that these curves remained almost identical when the devices were heated to 400°C, showing excellent temperature stability.

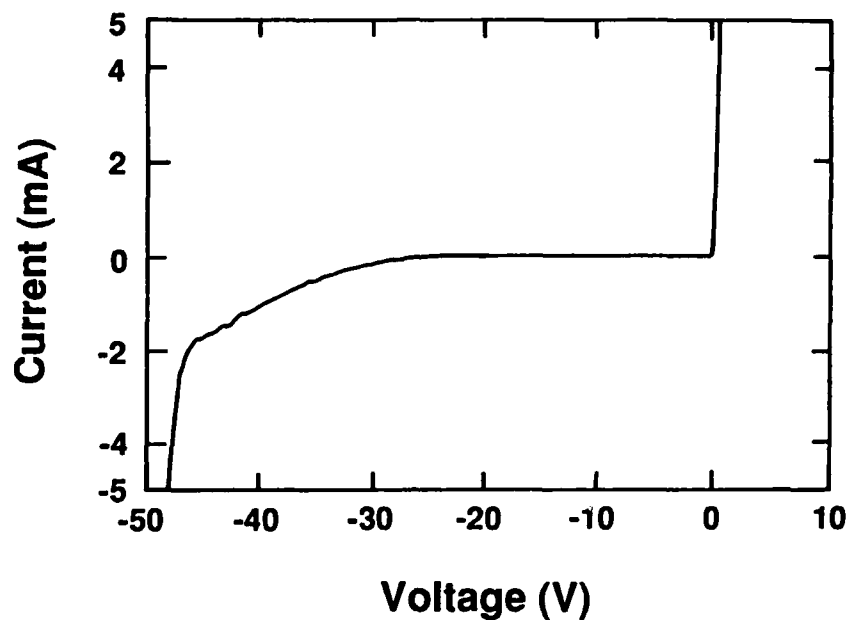


Figure 32: Current-voltage characteristics of an annealed Pt Schottky diode on n-type 6H-SiC with a carrier concentration of $n = 6 \times 10^{16} \text{ cm}^{-3}$.

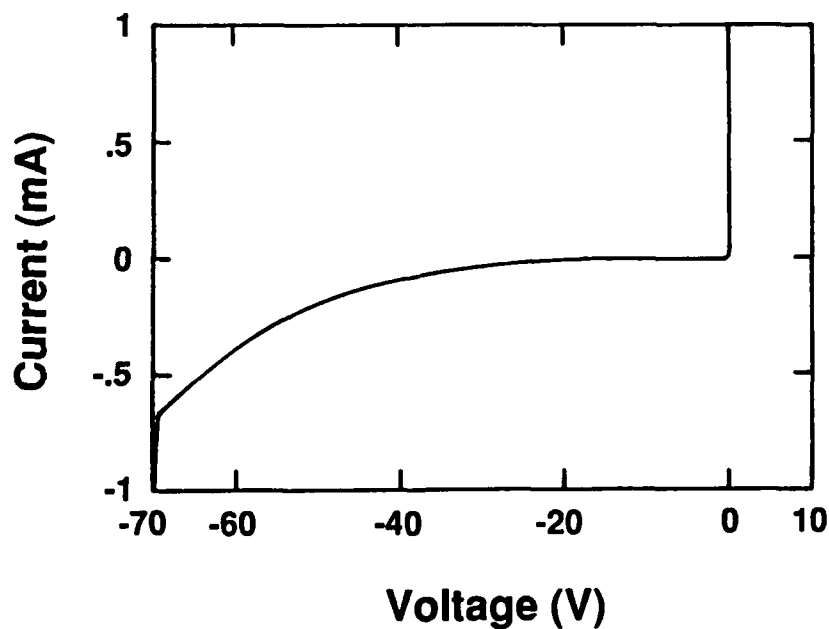


Figure 33: Current-voltage characteristics of an annealed Pt Schottky diode on n-type 6H-SiC with a carrier concentration of $n = 3.3 \times 10^{17} \text{ cm}^{-3}$.

VI. Gas-Source Molecular Beam Epitaxy of Silicon Carbide

A. Overview

The technique of molecular beam epitaxy (MBE) allows for precise control of growth parameters and minimization of sample contamination. The mean free path of source atoms or molecules at pressures used in MBE is much longer than the dimensions of the growth chamber. Intermolecular collisions within the growth chamber are unlikely. Parameters such as growth thickness can thus be controlled and reproducibly obtained using this technique. In the study described below, gaseous and thermally evaporated species will be provided to the growth surface.

B. Growth System

A schematic of the system to be used for gas-source MBE is shown in Figure 34. Samples are introduced into a small load lock chamber, the load lock chamber is evacuated, and samples are then transferred to the heating stage in the growth chamber. The load lock is used in order to increase sample throughput, as well as to keep the main deposition chamber under vacuum while samples are exchanged. It is pumped by a Balzers TPU 060 turbomolecular pump backed by a Sargent-Welch rotary vane pump. The load lock is operational, and pressures of 1×10^{-6} torr or below are easily reached in 30 minutes.

The growth chamber will be utilized for both *in situ* sample cleaning and deposition. Substrates will be cleaned prior to deposition by using an Ar^+ plasma to produce H^+ radicals from H_2 introduced into the system downstream from the plasma. The Ar^+ plasma will be obtained using an electron cyclotron resonance (ECR) plasma source developed in our laboratory[11]. This source is currently under construction in our machine shop. To date, no published work has been performed on plasma cleaning of $\alpha\text{-SiC}$. H^+ plasma cleaning of Si using this method has been achieved at 300°C [12].

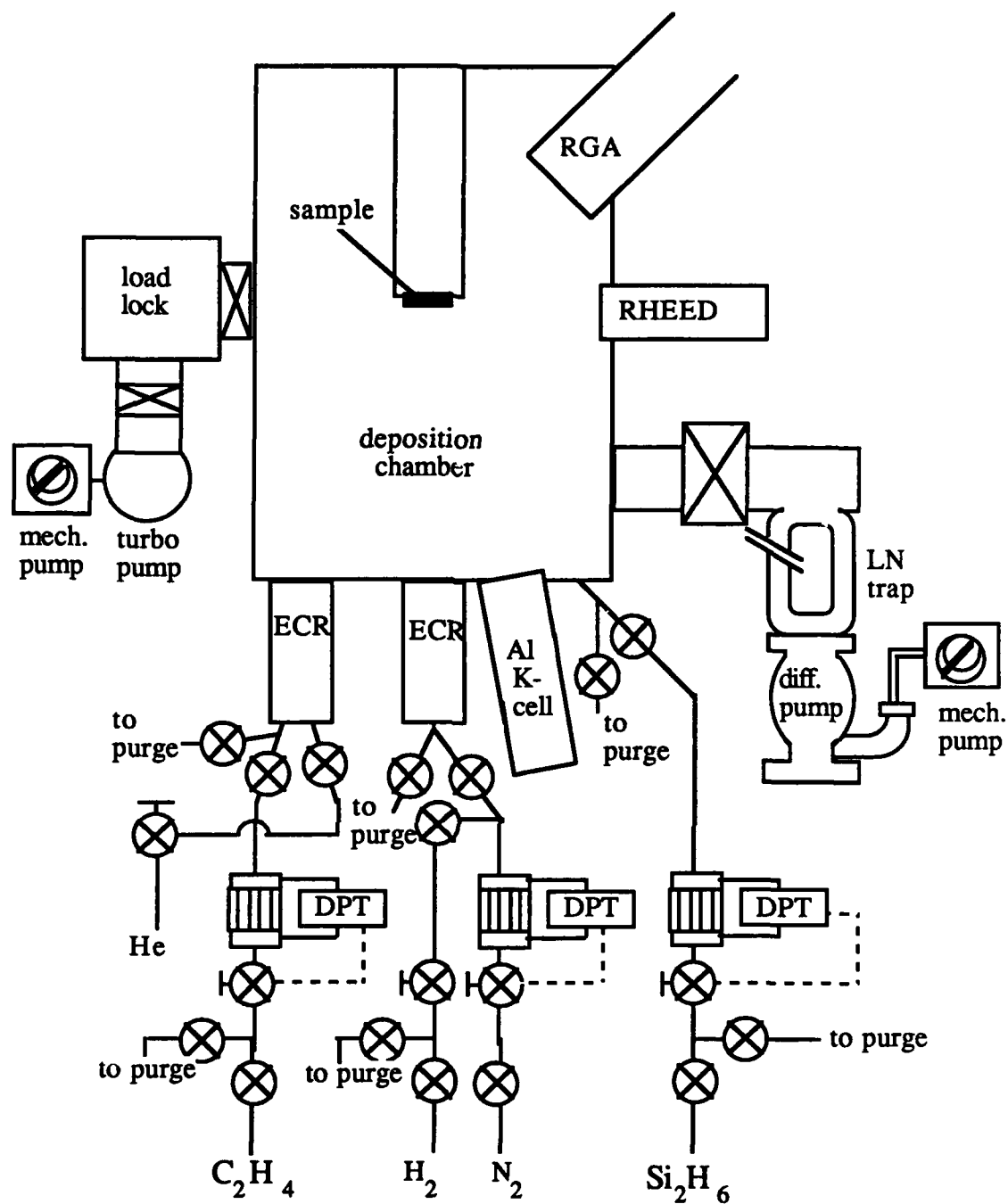


Figure 34: Schematic of Molecular Beam Epitaxy System

Samples will be heated using a heater designed for this system. Heat is produced by resistive heating of a coiled tungsten filament within a SiC-coated graphite cylindrical heating cavity lined with molybdenum and tungsten heat shielding. A high-purity pyrolytic BN disk is used as an insulating plate for holding the W coil. The heater shall be capable of temperatures of over 1000°C. Samples will be rotated during growth.

Species used in growth are introduced by way of the source flange. The source flange is equipped with ports for up to five solid sources and five gaseous sources. Disilane (Si_2H_6) will be used as a source of silicon, and will be supplied through a pressure-controlled flow system described in the next section. Ethylene (C_2H_4) will be used as a source of carbon. It will be introduced through a specially designed ECR plasma source. This source will enable the introduction of ethylene downstream of an induced Ar^+ plasma. Aluminum will be evaporated from a solid-source MBE effusion cell made by EPI Systems. Diatomic nitrogen (N_2) decomposed with an ECR source will be used as a source of nitrogen. Mechanical air-actuated shutters will be used with all sources to enable rapid switching between sources.

In the case of MBE, the distance between collisions for each molecule is much longer than the dimensions of the deposition chamber. This implies that flow is in the molecular regime, and flow rates are too low for standard mass flow controllers. A method of flow measurement and control has been developed which works well in the molecular regime[13]. It is based on the fact that in molecular flow, the conductance of a cylindrical tube is not a function of pressure. The mass flow, Q , through an element can be expressed as

$$Q = C\Delta P$$

where ΔP is the pressure difference and C is the conductance. The conductance of a cylindrical tube or series of cylindrical tubes in molecular flow can be accurately calculated. If the pressure difference across this element of known conductance

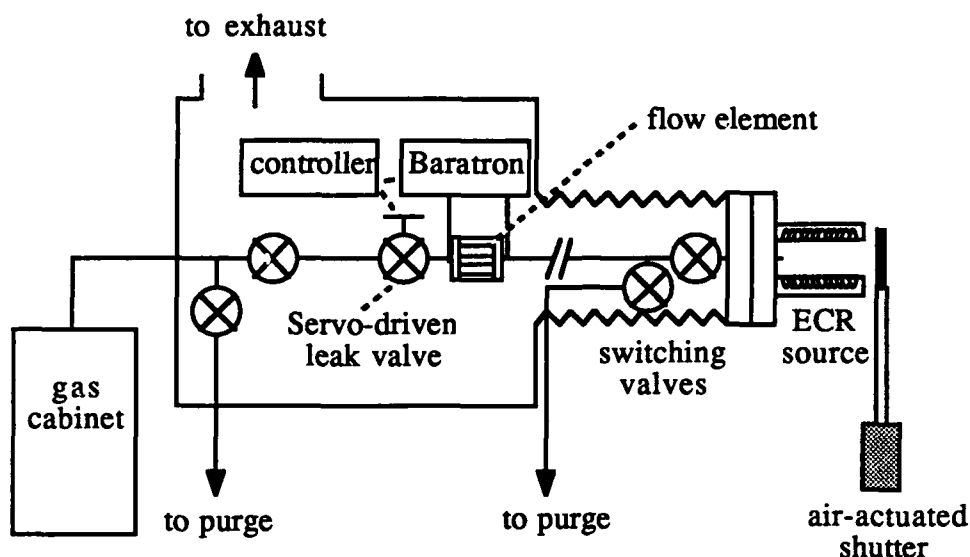


Figure 35: Valving System for Gaseous Sources

is measured, then the flow rate through this element can be easily found. The equipment used consists of a MKS CFE-0.5 precision molecular flow element, a MKS Model 120 differential capacitance manometer to measure the pressure difference across the element, and a Granville-Phillips Model 216 servo-driven leak valve and controller to control the gas flow to the element. The gas flow control system configuration is shown in Figure 35. Each gas used has its own flow control system. The entire flow control system, from the gas cabinet to the deposition chamber, will be exhausted for safety considerations. This type of system has been shown to enable the precise control of gas flow in the molecular regime, and can switch gases on in about 1 second and off in about 2 to 4 seconds[14].

The chamber also contains a UTI-100C mass spectrometer, which will be used in order to determine species present during growth. Characterization of films using RHEED during growth is also planned. The system is pumped using a Varian VHS-6 2400 l/s diffusion pump with a Vacuum Generators UHV liquid nitrogen cold trap backed by a rotary vane pump. Background pressures in the 10^{-10} torr range are obtainable in this system.

C. Discussion

Low temperature growth of high-purity, low defect-density, monocrystalline SiC layers on α -SiC substrates is the primary goal of this project. These SiC films will be grown on α -SiC substrates obtained from Cree Research described elsewhere in this report. Gases initially to be used for growth of SiC are disilane (Si_2H_6) as the Si source and ethylene (C_2H_4) for the carbon source.

The primary obstacle to low-temperature growth of SiC is the difficulty in locating a suitable source for monomolecular carbon. Several methods for the deposition of solid carbon have been considered. The most promising of these is resistive heating of a graphite filament[15]. If the filament is heated to around 2500°C , a significant flux of carbon leaves the sample due to thermal evaporation. The majority of C leaving the filament has been shown to be monomolecular in nature. This method has been utilized for carbon doping of GaAs in an MBE system. Huge amounts of power and a filament with very large cross-section would be necessary in order to obtain a flux sufficient for MBE growth of a binary carbide such as SiC. This fact precludes the use of this method at this time in this project. Other potential methods for solid-source deposition of C, such as laser evaporation and electron-beam evaporation, do not as yet yield large percentages of monomolecular carbon.

Gaseous sources of carbon such as hydrocarbons are relatively difficult to decompose. The growth temperature of SiC can be substantially lowered if the energy required for this decomposition can be decreased. One method which is useful in some instances is laser decomposition. High-energy monochromatic light, such as that produced by a laser, can impart sufficient energy to gaseous molecules to decompose them. Laser-enhanced chemical vapor deposition is a well-known technique for obtaining lower-temperature growth of many materials at pressures near one atmosphere. However, the efficiency of the decomposition process in the pressure range used in this research is extremely low.

Plasma decomposition is a proven method for low-temperature decomposition of gaseous species. The feasibility of an ECR source for monocrystalline growth of various materials in an MBE environment has been demonstrated[16,17]. Decomposition of ethylene will utilize a previously mentioned NCSU-developed ECR source modified to allow the downstream introduction of a gaseous species. Downstream introduction of a carbon-containing species is necessary because of the electrically conducting nature of carbon deposits on the inside of the microwave cavity. Argon gas will be used to sustain the plasma. Valving will be placed as close to the source as possible to minimize dead space and enable the rapid switching on and off of the ethylene supply.

In addition to SiC films, SiC/AlN pseudomorphic layers and solid solutions will also be grown as a part of this research. Al and N will also be used as the primary dopants in SiC. Suitable sources of Al and N are thus required for this research. Nitrogen will be obtained by ECR plasma decomposition of N_2 . MBE deposition of Al is possible either by thermal decomposition of an organometallic source, or thermal evaporation of solid Al using an effusion cell. Both types of sources are commonly used in molecular beam epitaxy.

However, thermal decomposition of triethylaluminum (TEAl) and trimethylaluminum (TMAI) at temperatures above 600°C has long been known to result in significant carbon concentrations in GaAs films[18]. A relatively unknown organometallic source, triisobutyl- aluminum (TIBAl) has been shown to result in much lower carbon concentrations in Al films relative to other alkyls[19]. However, carbon concentrations on the order of 0.1 percent in GaAs grown by gas-source MBE still result from temperatures in the 700°C range using TIBAl. This is undoubtedly too high for electrical applications of AlN. As a result, a solid-source effusion cell will be used for Al deposition.

Once all components are received and are in place, growth experiments will begin. First, characterization of plasmas obtained from both the C and N ECR sources

will be performed. Conditions will be optimized for plasma formation on both sources. Initial experiments will be run to determine optimum growth conditions for gas-source MBE of monocrystalline SiC on α -SiC. These will consist of varying substrate temperature and flow rates of Si and C source gases for growth on both the (0001) Si face and (0001) C face of 6H-SiC. Characterization of these films using electron and optical microscopy as well as electrical measurements will be performed. In addition, chemical analysis using secondary ion mass spectrometry (SIMS) may be performed to determine concentrations of trace impurities. Planned experiments also include eventual n- and p-type doping of SiC, growth of AlN, and growth of AlN/SiC solid solutions and pseudomorphic layers using gas-source MBE.

D. Conclusions

A system for growth of monocrystalline SiC thin films and SiC/AlN solid solutions and pseudomorphic structures using gas-source MBE has been designed and is nearing completion. This system consists of a loading chamber and a deposition/cleaning chamber. Samples will be cleaned prior to deposition using H^+ introduced downstream of an Ar^+ electron cyclotron resonance-induced plasma. The deposition chamber has the capability of using both solid and gaseous sources, and both will be used in this research. Gas flow will be controlled using a flow system based on measurement of the pressure drop across an element of constant conductance.

Gaseous sources are used for silicon, carbon, and nitrogen. Silicon will be deposited by thermal decomposition of disilane. Ethylene will be decomposed to an activated carbon-containing species using an electron cyclotron resonance plasma. Nitrogen will be decomposed using an ECR plasma. An MBE effusion cell will be used as a solid source for aluminum. Initial growth experiments should commence in the near future, as well as characterization of films grown by this process.

VII. Acknowledgements

The high frequency modeling work conducted by Cree Research was partially funded by Westinghouse Electric Corporation, Defense and Electronics Center.

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